SELECTIVE READ-OUT PROCESSOR

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OUTLINE

PART 1: OFF-DETECTOR ELECTRONICS

→ ECAL

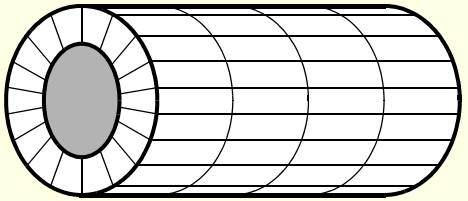
→ TASKS & ORGANIZATION

→ AREA & PERIMETER

THE CMS ELECTROMAGNETIC CALORIMETER

- **Frontend Electronics**
  - → 76832 crystals - electronic channels
  - → 10 samples @ 40 MHz bunch crossing frequency
- **Level 1 Trigger**
  - → Crystals form L1 trigger primitives: trigger towers
  - → 4032 trigger towers
- **Readout**
  - → 4 partitions: 2 EndCaps and 2 Half Barrels
  - → 5 x 5 = 25 crystals form a readout unit
  - → 3072 readout units

Half Barrel

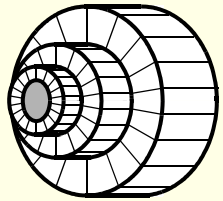


30600 Channels

1224 TTs **1224 RUs**

 = 

EndCap



7816 Channels

792 TTs **312 RUs**

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(see appendixes for segmentation)

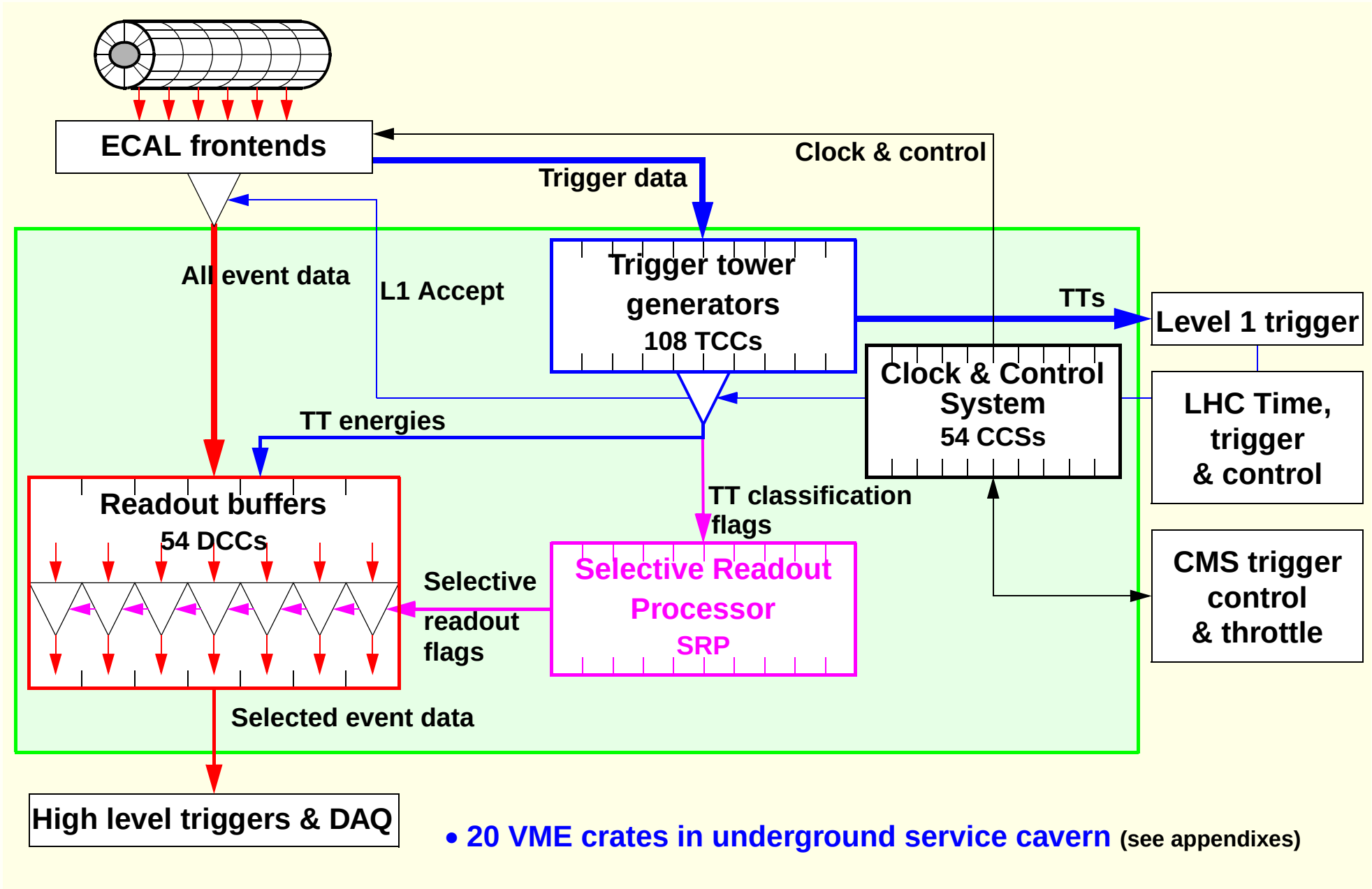
ECAL OFF-DETECTOR ELECTRONICS: TASKS AND ORGANISATION

- **Control**
  - → Interface to Time, Trigger and Control (TTC) system of LHC
  - → Interface to Trigger Control and Trigger Throttling Systems of CMS
  - → Configuration and control of frontends
    - → 54 CCSs (Clock and Control System boards, CERN)

- **Level 1 Trigger**
  - → Receive trigger data from frontends
  - → Form trigger primitives *i.e.* trigger towers
  - → Transfer trigger tower data to L1 trigger
    - → 108 TCCs (Trigger Concentrator Cards, LLR)

- **Readout**
  - → Receive L1 accepted event data from frontends
  - → Extract relevant calorimeter data according to some selection criteria
  - → Transfer selected data to High Level Triggers and DAQ system
    - → 54 DCCs (Data Concentrator Cards, LIP) + SRP (Selective Readout Processor, Saclay)

CMS ECAL OFF-DETECTOR ELECTRONICS: AREA AND PERIMETER



- **20 VME crates in underground service cavern** (see appendixes)

PART 2: SELECTIVE READ-OUT PROCESSOR

→ MOTIVATION AND GOALS

→ SELECTIVE READ-OUT ALGORITHMS

→ FUNCTIONAL DESCRIPTION

MOTIVATION AND GOALS

- **CMS DAQ capabilities**
  - → **Total event size: 1 Mbyte**
  - → **Allowed average ECAL event size: 100 Kbyte**
  - → **Data throughput: ~100 Gbyte/s**

- **Raw data volume of ECAL per event: 1.5 Mbyte**
  - → **ECAL raw event size exceeds total CMS event size**
  - → **At 100 kBq L1 Trigger rate ECAL data bandwidth of 150 Gbyte/s > DAQ throughput**

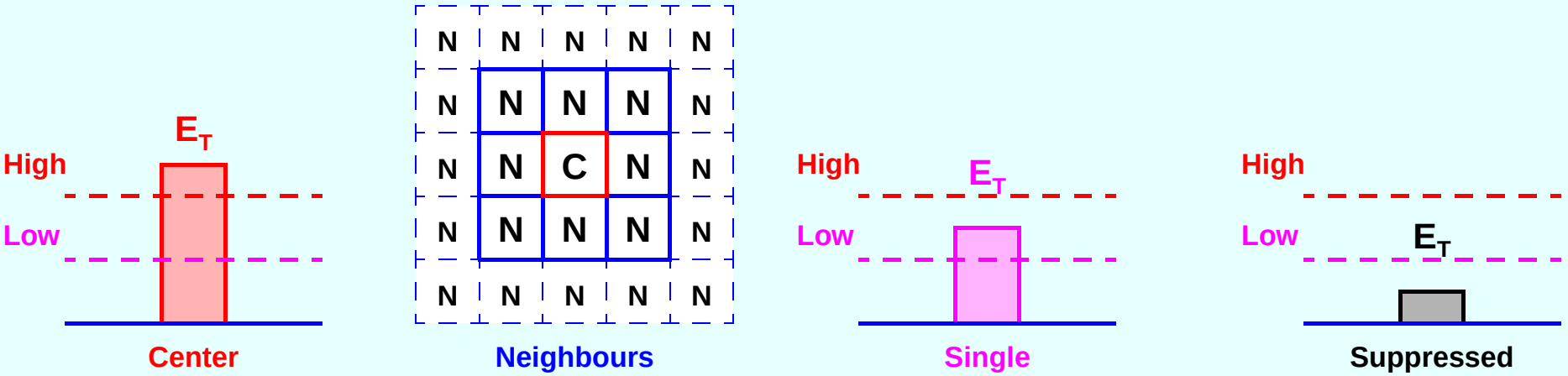
Reduction factor of almost 20 is necessary

- **Crystal-by-crystal zero suppression : non-linearity and degraded energy resolution**

- **Selective readout:**
  - → **Define zones of interest on event-by-event basis**
  - → **Read full precision data from channels within these zones of interest**
  - → **Zero suppress the rest of channels**

A TYPE OF SELECTIVE READ-OUT ALGORITHMS

- **Considered classification of Trigger Towers**



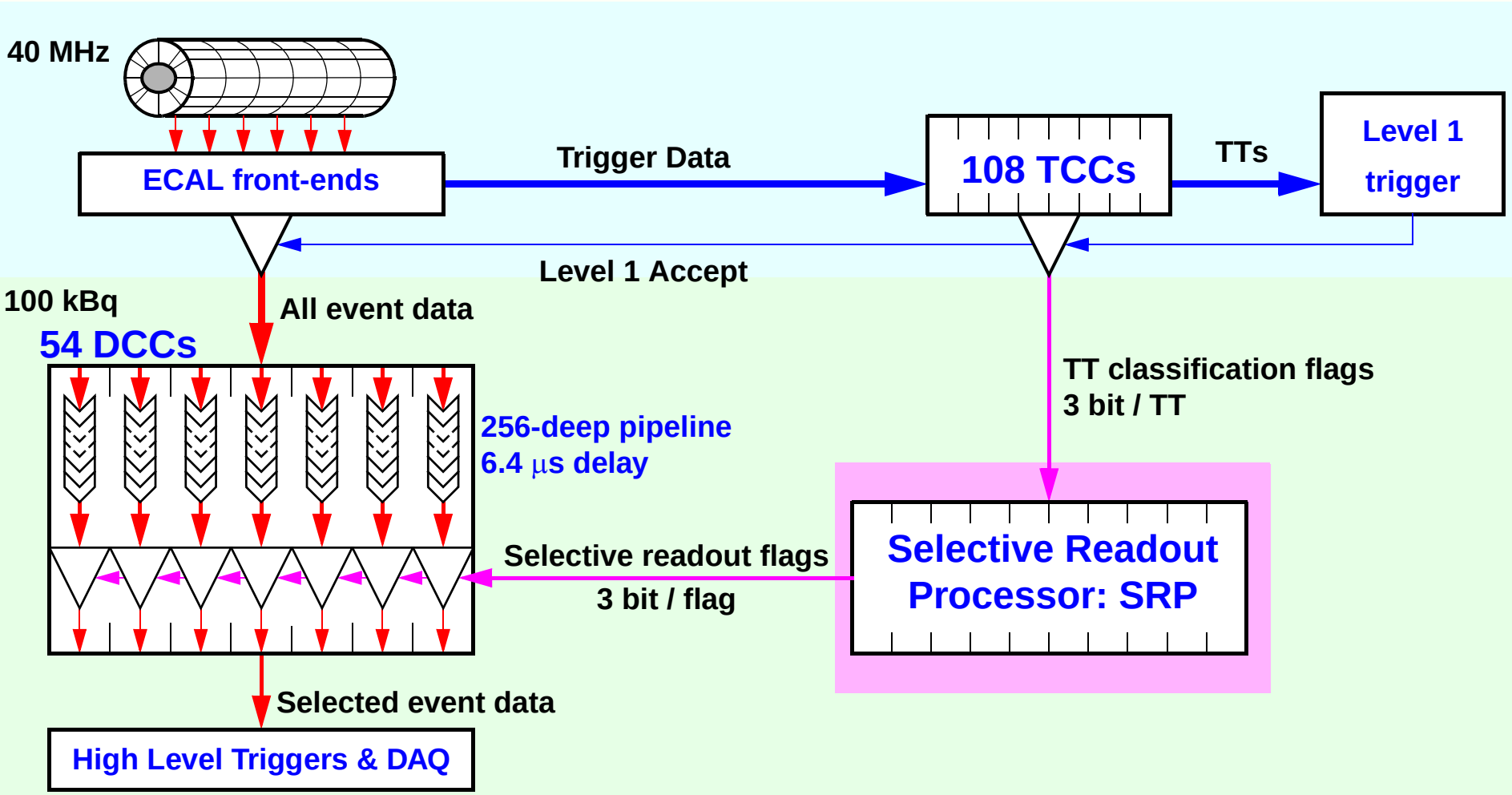
- **Applied read-out algorithms**

		Scheme A	Scheme B
High Threshold (GeV)		2.0	5.0
Low Threshold (GeV)		0.6	2.5
Action	Centre	ZS (0σ)	All Data
	Neighbour	ZS (0σ) in 3x3	All Data in 3x3 or 5x5
	Single	ZS (0σ)	All Data
	Suppressed	No data	ZS (3.5σ)

- **Possibility to achieve necessary data reduction factor - shown** (see appendixes)

→ **Note: ECAL is always entirely read with coarse granularity data (*i.e.* energy deposited in TTs)**

FUNCTIONAL DESCRIPTION



- 108 input links from TCCs
- 54 output links to DCCs
- 1.6 Gbit/s links
- 100 kBq asynchronous operation
- Processing latency budget ~3-5 μs

→ VME cards of custom FPGA based hardware

PART 2: ARCHITECTURE

→ ADOPTED ARCHITECTURE

→ SRP INTERFACES

→ TARGETED LAYOUT OF SRP BOARDS

→ SRP TESTBED

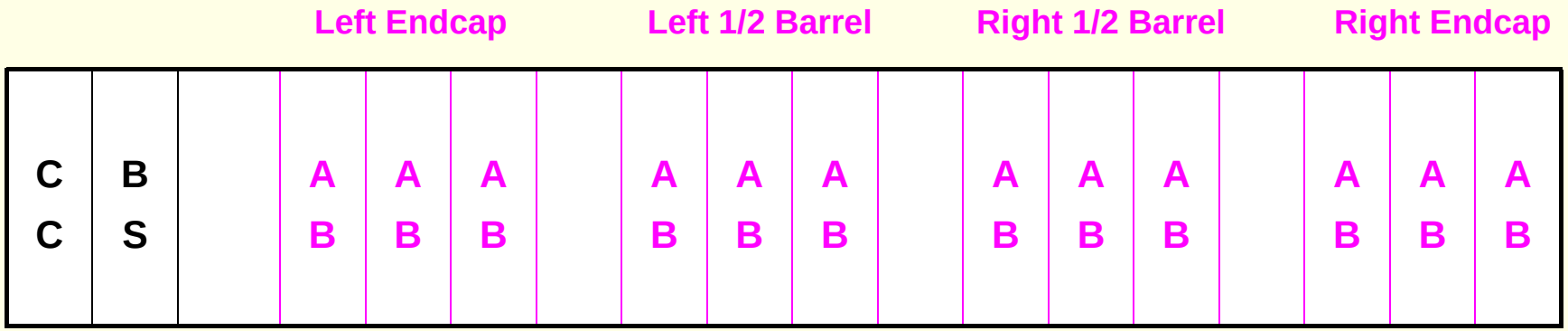
ADOPTED ARCHITECTURE

- **Single 6U VME64x Crate**

- **12 Algorithm Boards (AB)**
  - → **following 4 ECAL partitions**
  - → **3 AB per partition**

Only one custom board to develop and maintain

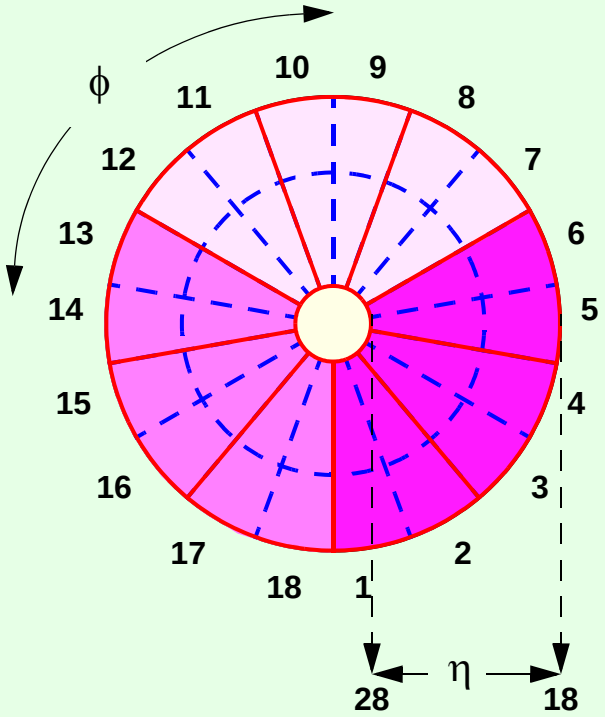
- **Crate Controller (CC) and Boundary Scan (BS) controller**
  - → **"Standard ECAL"**

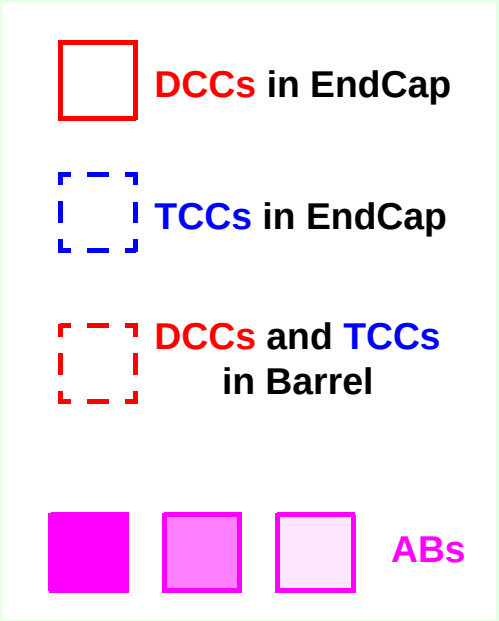


MAPPING OF TCCS, DCCS AND ABS

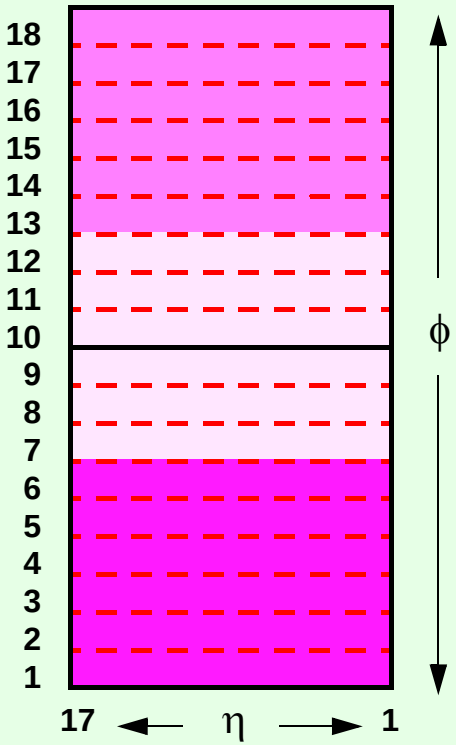
- **EndCap: 40° φ sectors with 1 DCC and 4 TCCs**
- **Half Barrel: 17η x 20° φ Super Modules with 1 DCC and 1 TCC**

EndCap





Half Barrel



9 DCCs, 36 TCCs, 3 ABs

3 DCCs & 12 TCCs per AB

18 DCCs, 18 TCCs, 3 ABs

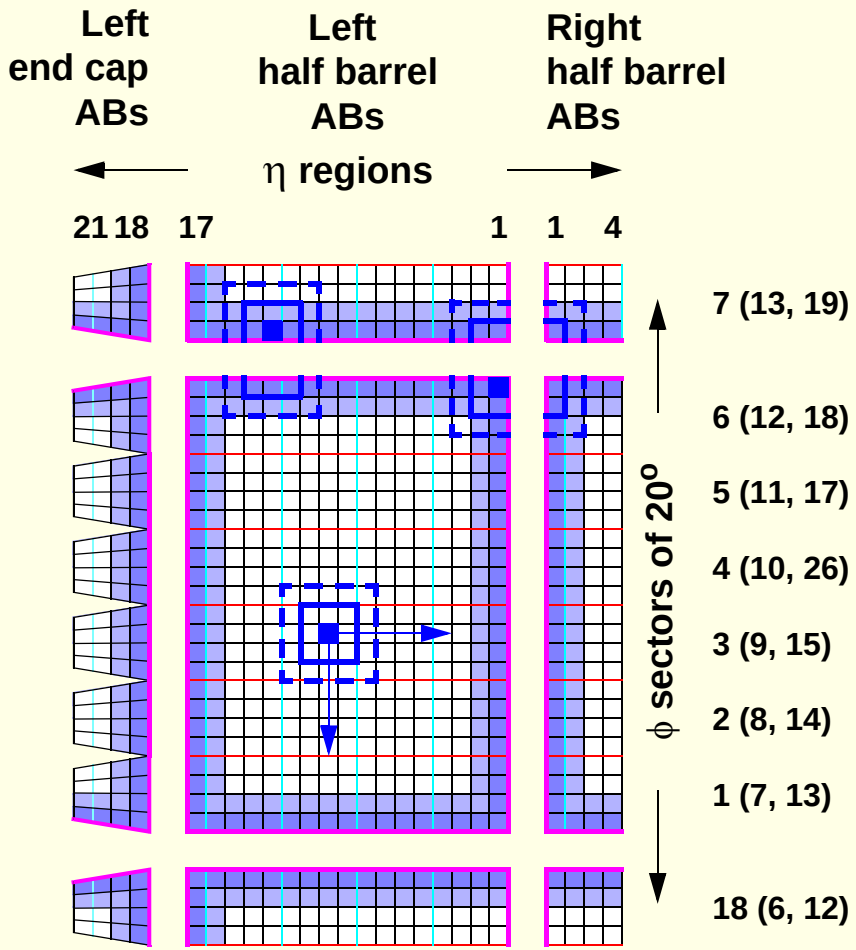
6 DCCs & 6 TCCs per AB

Algorithm Boards

- **Selective read-out algorithm**
  - → 3 x 3 or 5 x 5 windows slide across η-ϕ grid
  - → TTs are classified according their energy
  - → Selective read-out flags are derived accordingly

- **The windows cross Algorithm Board boundaries**
  - → ABs exchange information about TTs on their edges
  - → Exchanged data is enough for 9x9 sliding windows

- **Example of a Barrel AB**



SRP INTERFACES

- **With external systems: Trigger Control System and Run Control**

  → **CMS standard solutions have been adopted**

- **With other OD Electronics components**

  → **Receives TT classification flags from 108 TCCs** **up to 12 TCCs / AB**

  → **Exchange boundary TT classification flags among ABs** **up to 8 ABs / AB**

  → **Sends SR flags to 54 DCCs** **up to 6 DCCs / AB**

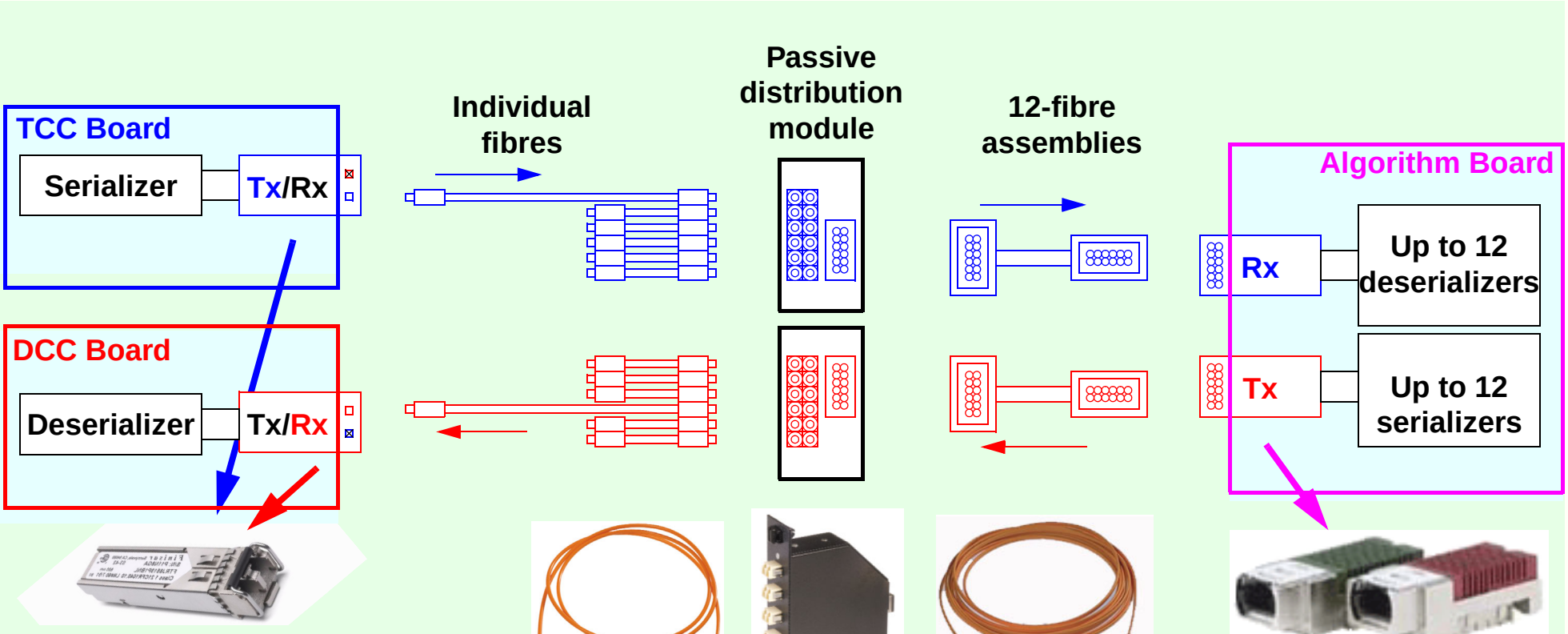
- **Optical communication links have been adopted**

  → **allows for high speed connections : 1.6 Gbit/s**

  → **alleviates potential problem of distances between ODE components**

  Parallel optic technology for high density design

SRP COMMUNICATIONS: TCC - AB - DCC CHANNELS



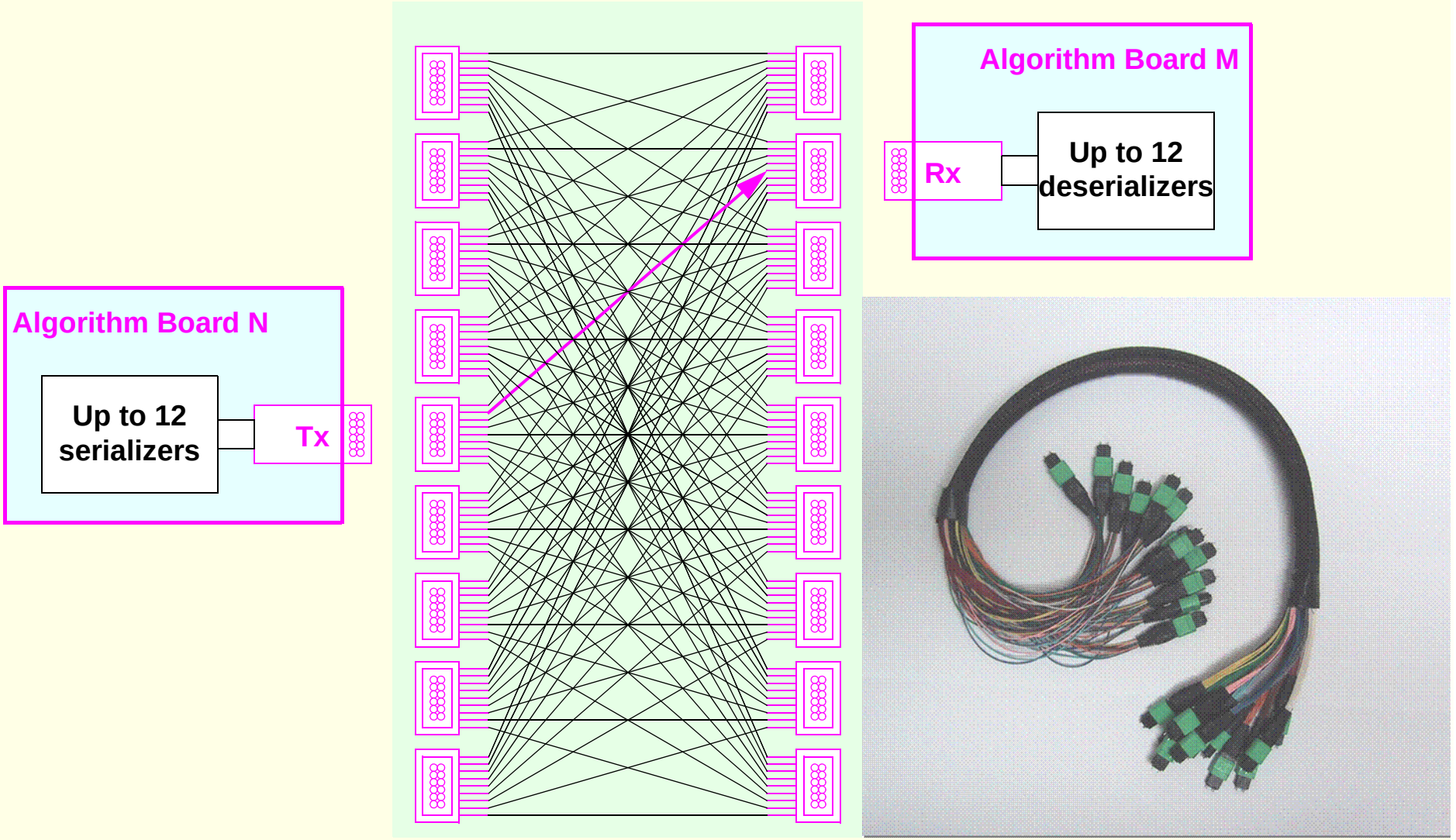
Optical Transceivers
Small Form factor Pluggable (SFP)
with Lucent Connector (LC)

Parallel Optic
12-Channel MPO
Rx and Tx Pairs

- **SFP and MPO pluggable devices relative freedom in choice of**
  - → **Manufactures (multi source agreement)**
  - → **Data rates without changing PCBs**

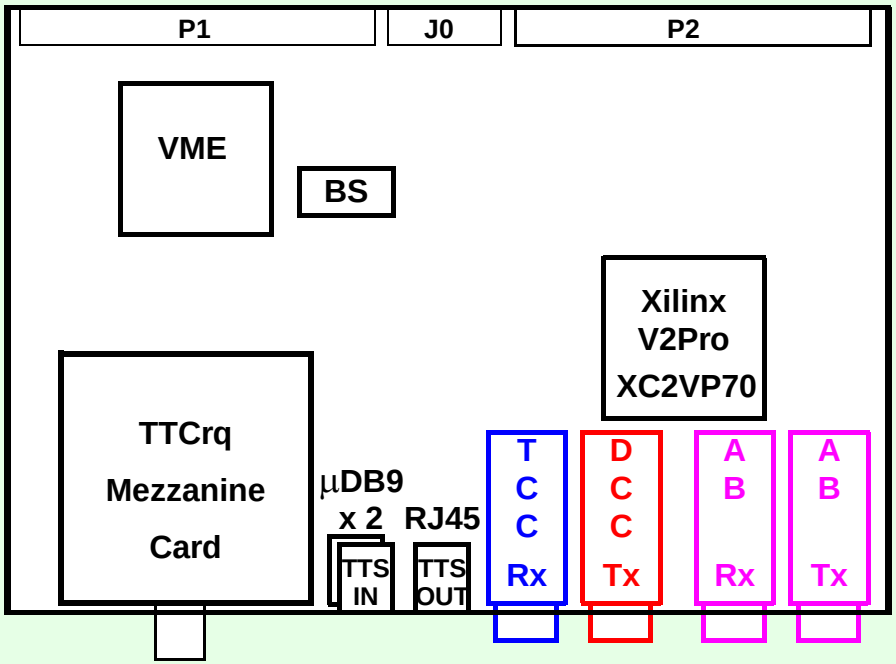
SRP COMMUNICATIONS: AB - AB CHANNELS

- **Passive optical cross-connect for all-to-all AB connectivity**



TARGETED LAYOUT OF THE ALGORITHM BOARD

- **6U single slot VME64x board**
  - → "ODE standard" VME interface
  - → TTCrq "standard" TTC interface
  - → 2 pairs of parallel optic modules
  - → 2 μDB9 connectors for TTS signals from neighbour ABs
  - → RJ45 connector for TTS interface
  - → Boundary scan and JTAG

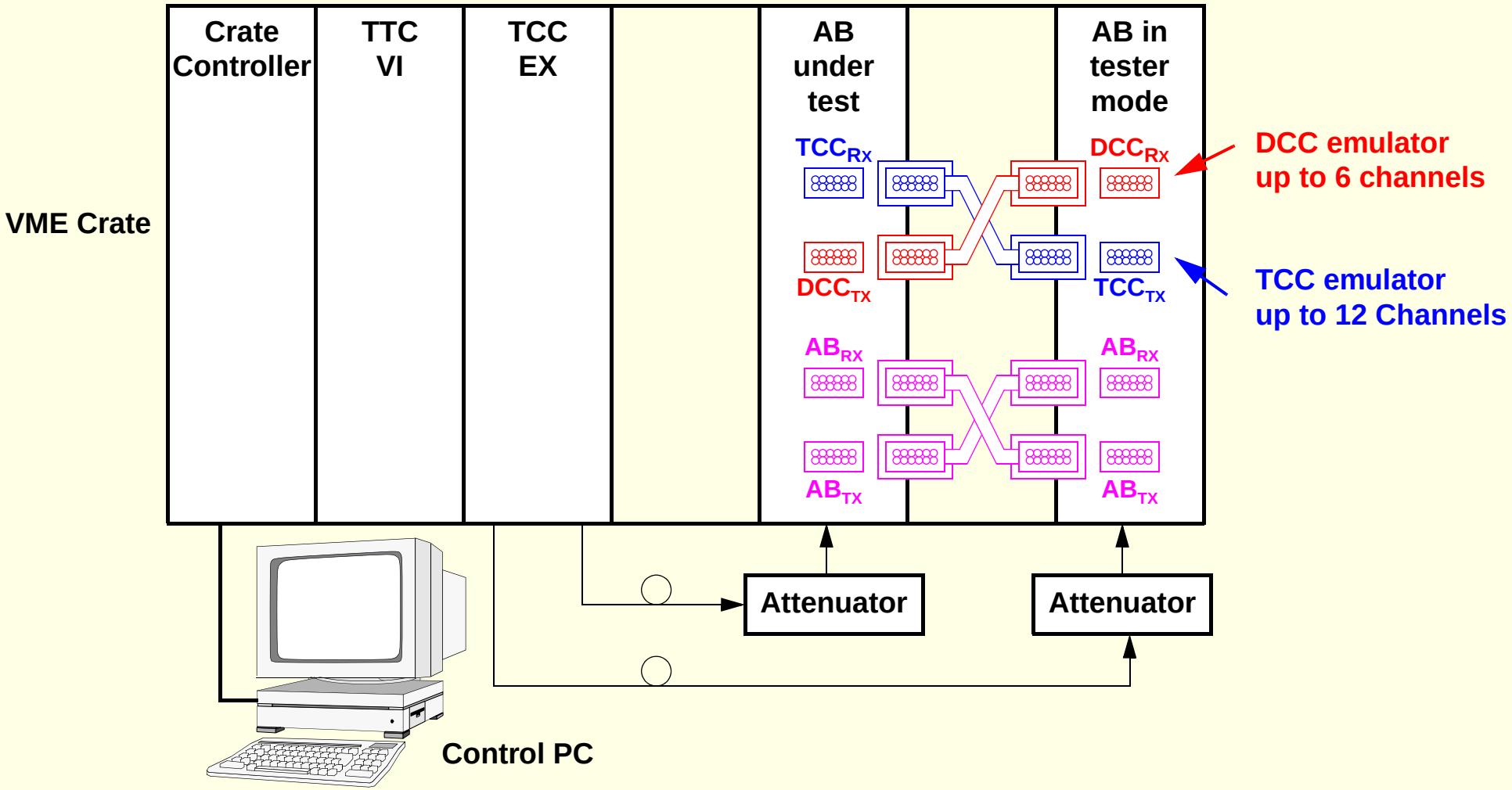


- **Xilinx Virtex2Pro FPGA XC2VP70-6FF1704C**
  - → Selective Readout Logic
  - → 20 serial transceivers with up to 3.5 Gbit/s (RocketIO)
    - up to 12 for TCC / DCC unidirectional connections
    - up to 8 for AB bidirectional connections
    - 8b / 10b coding, framing and CRC calculation
  - → Embedded PowerPC processor: can be used for monitoring purposes

SRP TESTBED

- **Debugging and testing Algorithm Board with Algorithm Board**

  → **Dedicated firmware for AB tester mode**



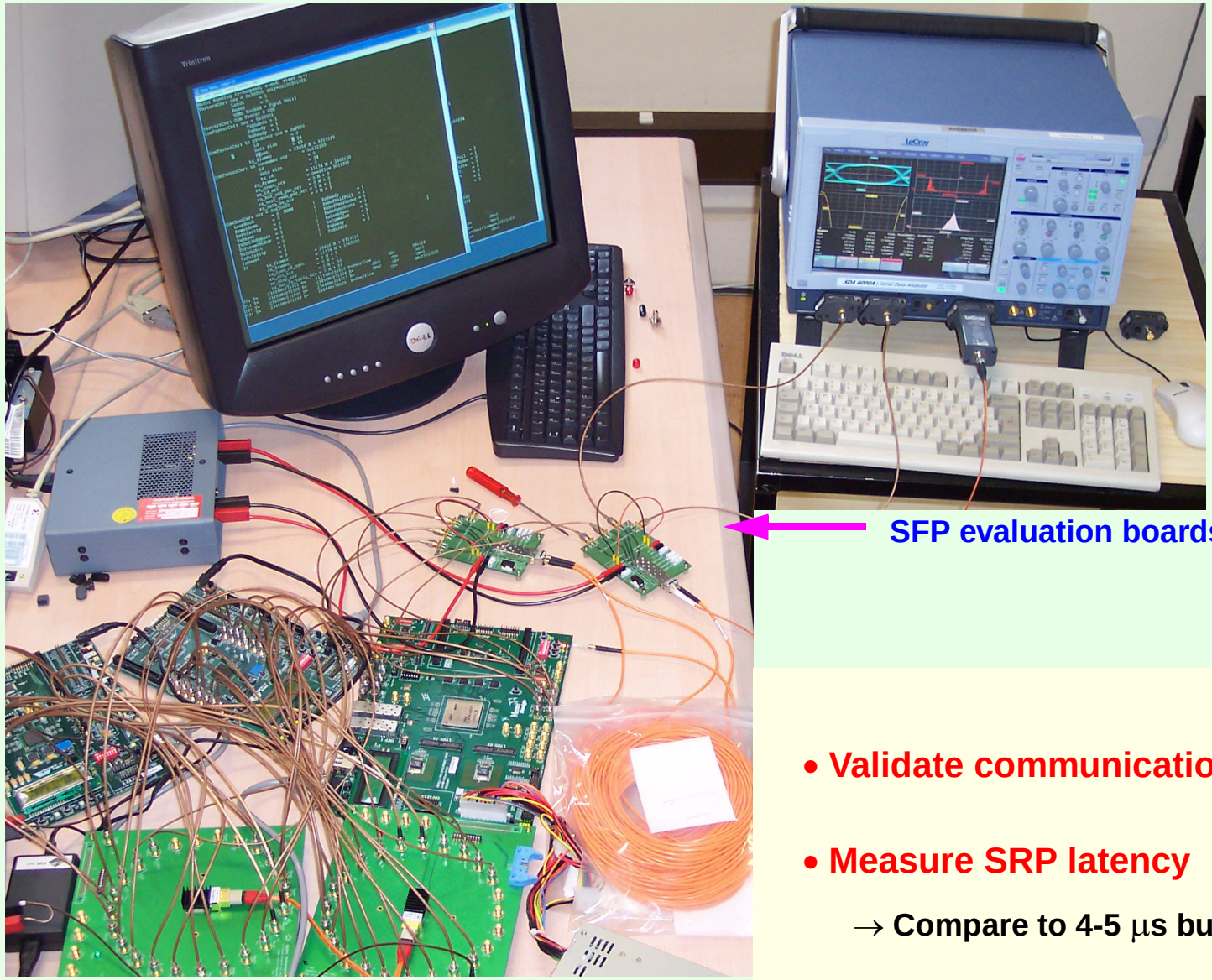
PART 3: CONDUCTED SYSTEM IMPLEMENTATION PRESTUDIES

→ COMMUNICATION R&D

→ SYSTEM R&D

SETUP FOR IMPLEMENTATION R&D WORK

Consoles for embedded PowerPCs



LeCroy Serial Data Analyser

SFP evaluation boards

Xilinx Virtex2Pro development boards

Parallel optic evaluation boards

- **Validate communication channels**
- **Measure SRP latency**

  → **Compare to 4-5 μs budget**

COMMUNICATION R&D: STATUS

- **Gained experience with Xilinx RocketIO and embedded PowerPC processor**

- **Communication R&D**

  → **Validated TCC-SRP-DCC communication protocol**

  → **Verified inter-operability between parallel optic Tx and Rx modules and SFP transceivers**

  → **Achieved operation of fully loaded parallel optic modules : 12 x 2.5 = 30 Gbit/s**

  → **No errors on link or application levels during 8 h / per day**

  → **Measurements on LeCroy scope show BER far below 10^{-12}**

  (BER of 10^{-12} corresponds to a "theoretical" packet loss probability of 1 per 23 days)

  (Data losses does not result in TCC-SRP-DCC synchronisation loss)

  → **3.5 dB for worst case optical power attenuation despite of cable plant with at most 4 connectors**

  → **Jitter budget is satisfied**

SYSTEM R&D: PROTOTYPING WITH VIRTEX2PRO EVALUATION BOARD

- **Firmware: simplified but enough representative model of AB**
  - → including TTC, TCC and DCC emulator models
- **AB model**
  - → Serves only one barrel SM
  - → Exchanges boundary data with two neighbour ABs
  - → Exchanged data is enough to perform 9x9 sliding window algorithm
  - → Implemented SR Algorithm uses 3x3 windows
- **Total latency measurements**
  - → From L1Accept received by TCC Emulator to SR Flags received by DCC Emulator
  - → 252 clock cycles
  - → Measurements done with 125 MHz clock : ~2 μs

Confidence that timing requirements can be met

PART 4: DISCUSSION

→ PLANNING AND BUDGET

→ RISKS

→ REFERENCES

PLANNING AND BUDGET

- **Prototype Algorithm Boards**
  - → **Design and production: May - December 2004**
  - → **2 prototypes will be assembled for mutual debugging**
  - → **Debugging and tests start in January 2005**
- **System-wide TCC-SRP-DCC tests: from April 2005 in CERN**
  - → **Possible earlier inter-operability tests**
- **Production of final ABs: September - December 2005**
  - → **Produced 12 active + 6 spares**
  - → **Tested all 6 barrel ABs**
- **Commissioning of SRP: from January 2006**
- **SRP budget estimated to 300 kCHF**
  - → **Including fibre optic components and cables for TCCs and DCCs**

RISKS

- **Obsolescence of fibre optic components**
  - → **Pluggable: easy to replace**
  - → **SFP MSA - multitude of producers - long life cycle expected**
  - → **Parallel optic MSA - at least 3 sources: Agilent, Picolight, Zarlink**
  - → **Spares of parallel optic modules > spares of Algorithm Boards**

- **Performance increase or functional modifications**
  - → **Communication links can go up to 2.5 Gbit/s**
  - → **Exchanged between AB cards data will be enough to perform 9x9 sliding window algorithm**
  - → **There is a spare bit in 3 TT classification and SR flags (giving 4 additional classification codes)**
  - → **Occupation of 2VP70 FPGA estimated to 60-70%**
  - → **FF1704 package compatible with 2VP70, 2VP100 and 2VP125 Xilinx FPGAs**

REFERENCES

- **SRP system R&D studies**

  http://cmsdoc.cern.ch/~jlfaure/OD_Web_Folder/November-03/031113_SRP_status.pdf

- **Communication R&D studies**

  http://cmsdoc.cern.ch/~jlfaure/OD_Web_Folder/Q2_2004/040427_cern_prep_esr.pdf

- **Interface with TCS**

  http://cmsdoc.cern.ch/~jlfaure/OD_Web_Folder/Q1-2004/040302_irakli_status.pdf

PART 5: APPENDIXES

→ ECAL SEGMENTATION IN TTS AND RUS

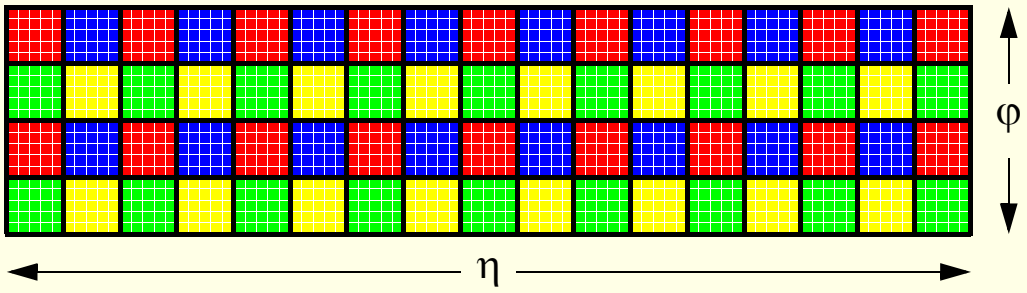
→ RACKS AND CRATES OF OD ELECTRONICS

→ SELECTIVE READ-OUT ALGORITHM STUDIES

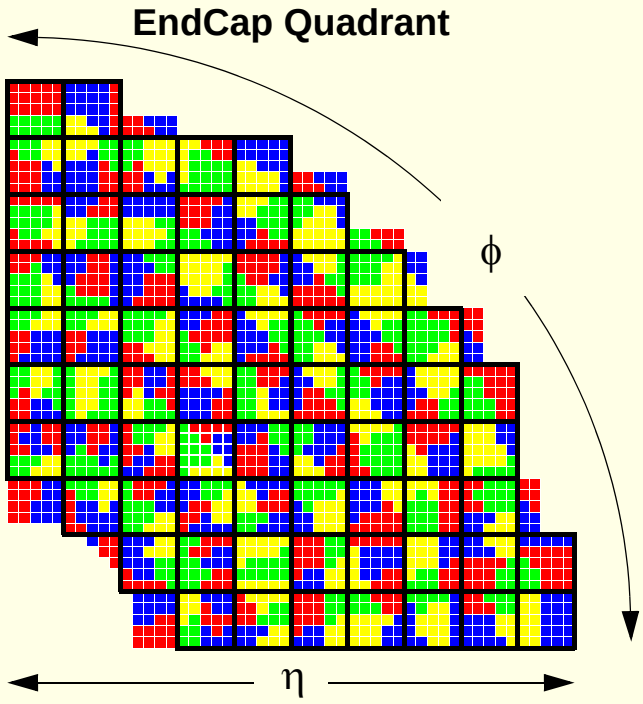
ECAL SEGMENTATION IN TRIGGER TOWERS AND READ-OUT UNITS

- **In Barrel**
  - → **Trigger Tower and Readout segmentation in η-φ coordinates**
  - → **Trigger Tower = Readout Unit**
- **In EndCap**
  - → **Trigger Tower segmentation in η-φ coordinates**
  - → **Read-out segmentation in x-y coordinates**

Barrel Super Module



EndCap Quadrant



CRATES FOR OFF-DETECTOR ELECTRONICS

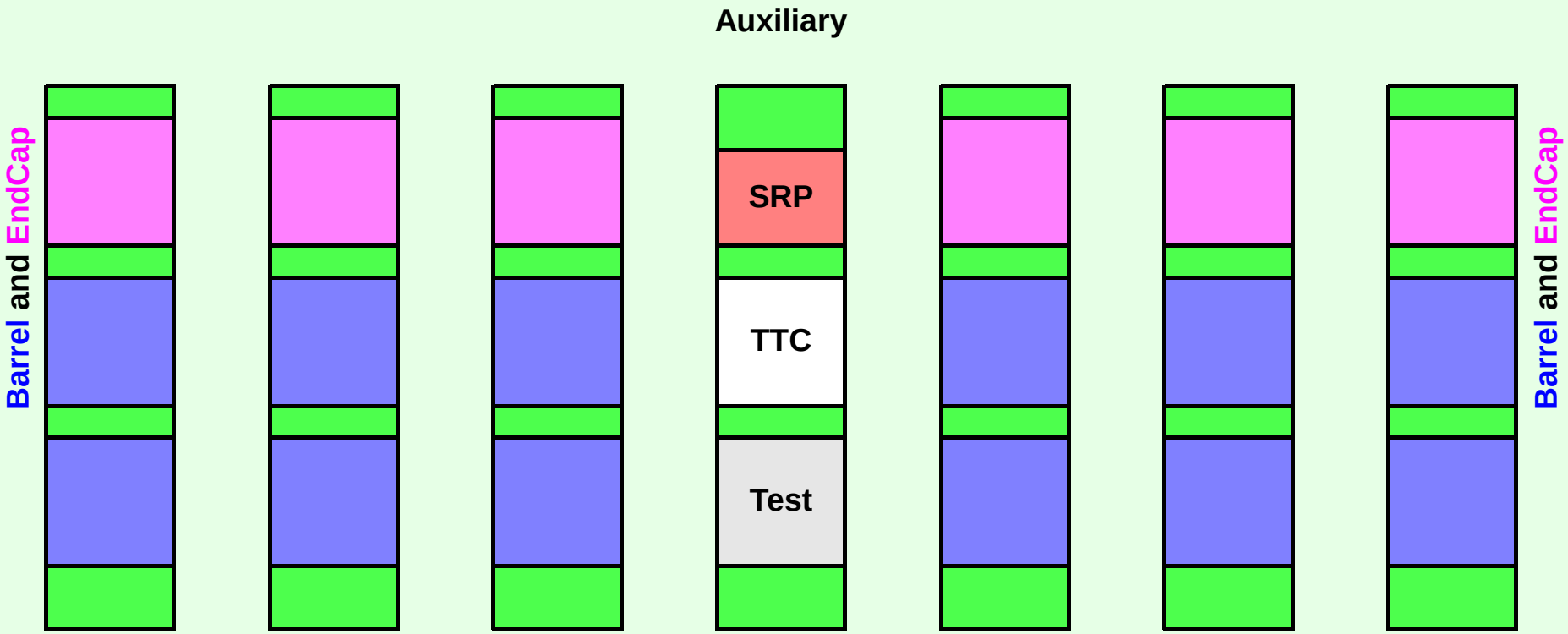
- **21 VME crates are housed in 7 racks**

  → **18 9U crates for CCS-DCC-TCC**

  → **1 6U crate for SRP**

  → **1 9U crate for TTC**

  → **1 9U crate for Test (optional)**



- **Barrel and EndCap crates are mixed in racks in order to minimize cable length**

CRATES FOR OFF-DETECTOR ELECTRONICS

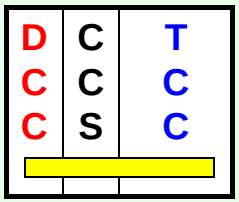
- **Off-Detector Electronics is housed in VME crates**

  → **Each crate is interfaced to run control via a Read-out Crate Supervisor - ROCS:**

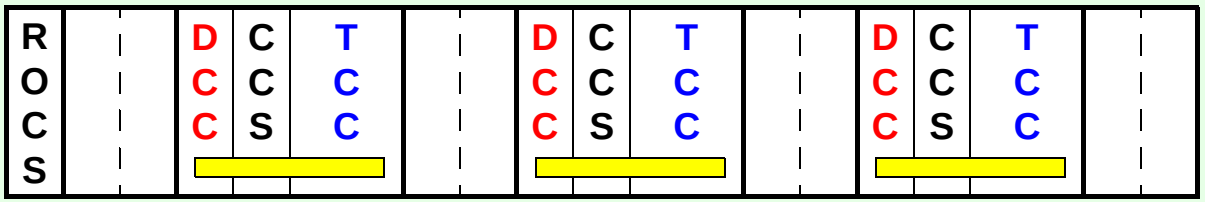
  PC + VME interface

- **Barrel crates**

Super Module DAQ Unit

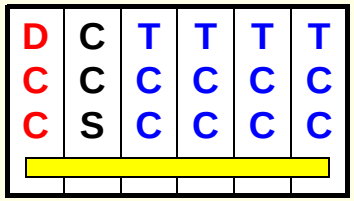


6 Read-Out Crates per Half Barrel

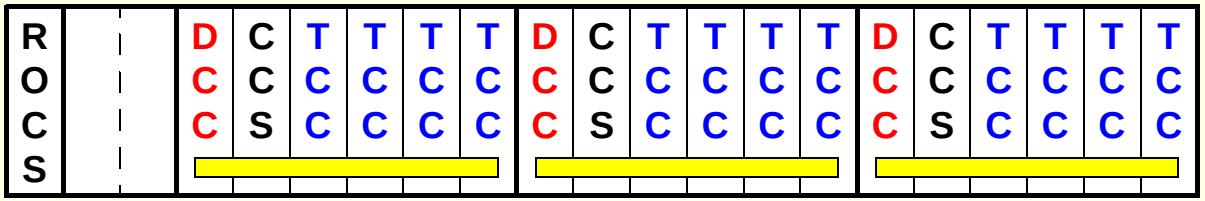


- **EndCap crates**

40^{o} DAQ Unit



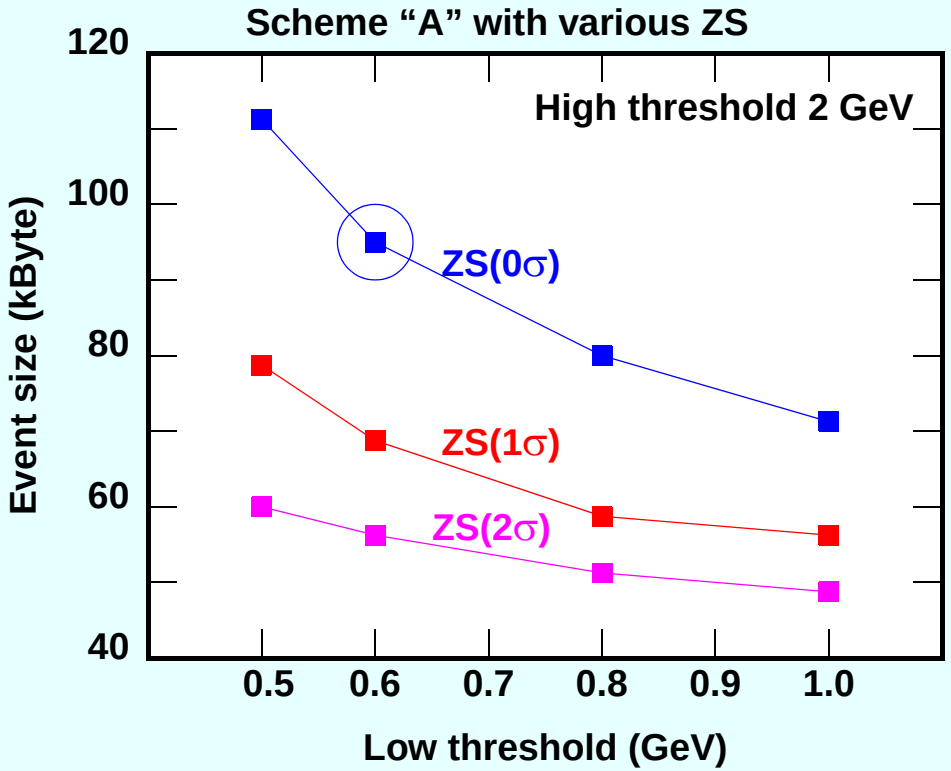
3 Read-Out Crates per EndCap



SELECTIVE READ-OUT ALGORITHM STUDIES

- **Feasibility to achieve desirable reduction factor shown**

  → **Example from *N. Almeida, J. Varela, CMS IN 2002/009***



ORCA jets with p_T within 50-100 Gev

plus 17 minimum bias events

- **Avoiding non-linearity and degradation of energy resolution compared to simple ZS**

  → **See for example *R. Rutherford, CMS IN 2003/001***

- **Work to update ORCA code and further studies of SR algorithms ongoing**