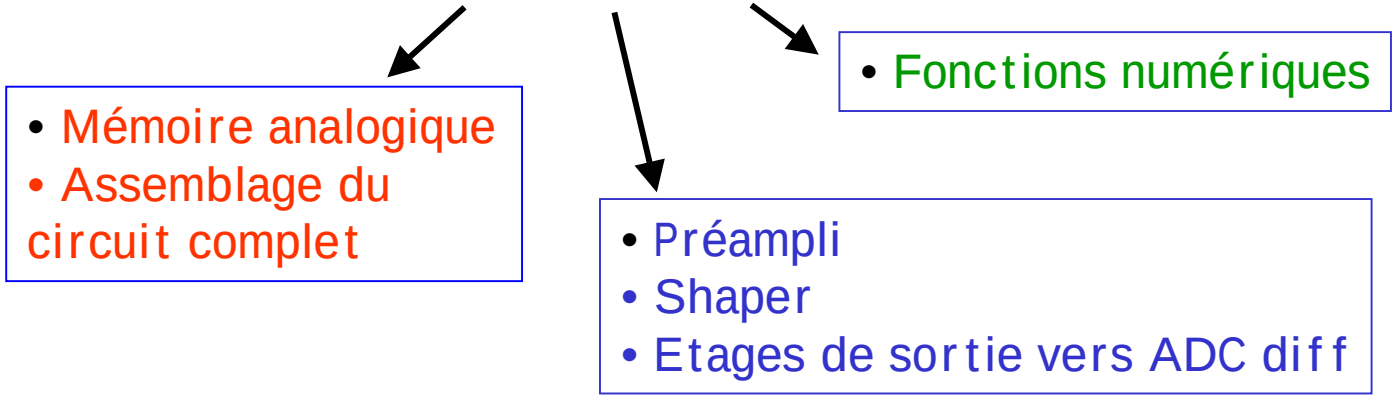
Quoi de neuf depuis Villié-Morgon 2002 ?

❑ Asics Pace3 Preshower

- Poursuite de la participation à la migration DMILL → IBM 0.25µm
- Codéveloppement CERN / IPNL / RAL



- Participation à la caratérisation des circuits Q2/03 (test board au CERN)
- Circuits fonctionnels et performances analogiques atteintes au 1er run
- Redesign du contrôleur I2C (fonction numérique) en juin 2003
- Ajout d'hystérésis sur les entrées numériques de contrôle

Quoi de neuf depuis Villié-Morgon 2002 ?

❑ ASIC récepteur de ligne LVDS (ECAL VFE)

- Localisation: carte VFE ECAL
- Circuit tampon entre ADC1240 et concentrateur numérique FENIX

- ASIC 0.25µm
- conception CERN + CHIPIDEA
- Entrée analogique différentielle
- Sorties numériques LVDS
- 4 ADC en 1

- Gros ASIC numérique
- 0.25µm
- Nb I/O > 140
- Entrées CMOS

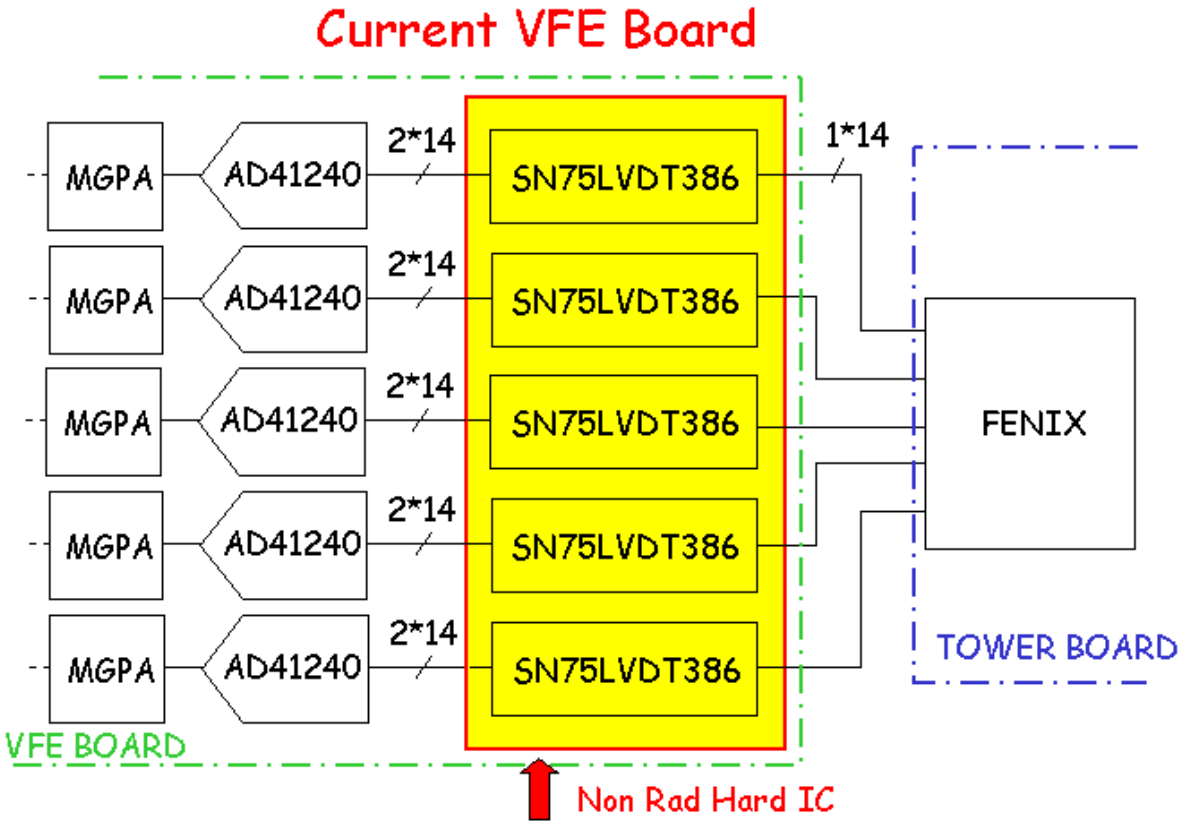
Buts:

- Abaisser le coût AD9042
- Modif architecture VFE
- Diminuer la puissance globale

ASIC LVDS_RX

BUT

• Remplacer le circuit commercial TI utilisé sur la carte VFE 2003 par un circuit durci

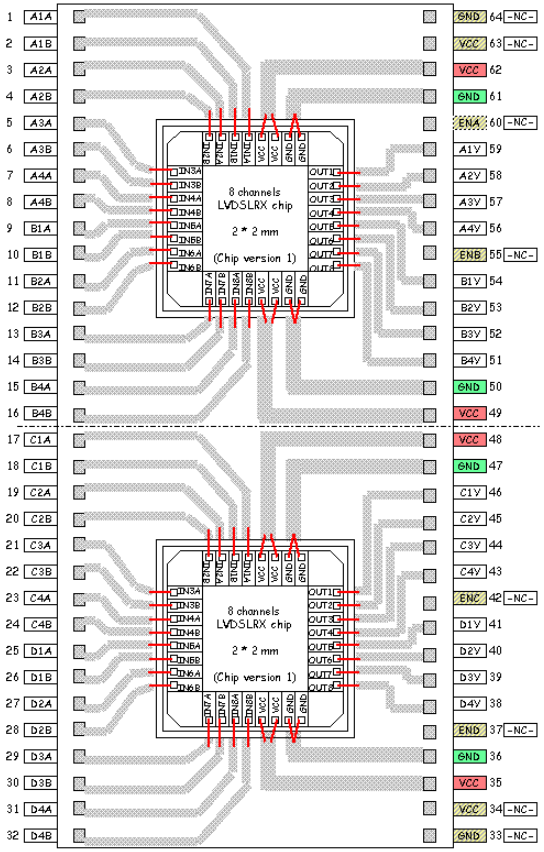


LVDS_RX: Options de design

1. Circuit pin to pin compatible circuit TI, boitier TSSOP68, 1 seule chip
   → Non retenu:
   - trop de silicium perdu

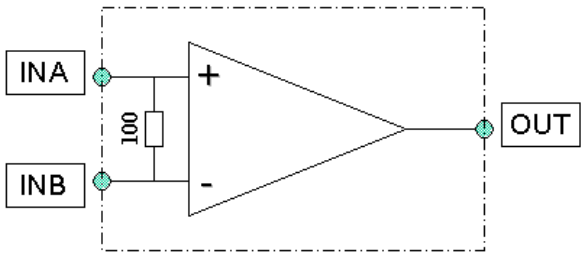
2. Circuit pin to pin compatible boitier TSSOP68, 2 chips, 2 cavités
   → Non retenu:
   - Pas d'assembleur volontaire pour design d'un leadframe custom
   - Volume de production trop faible

3. Option retenue:
   - Circuit 8 voies, MPW avec service chips CMS
   - Boitier low cost LPCC32 ASAT
   - Redesign carte VFE



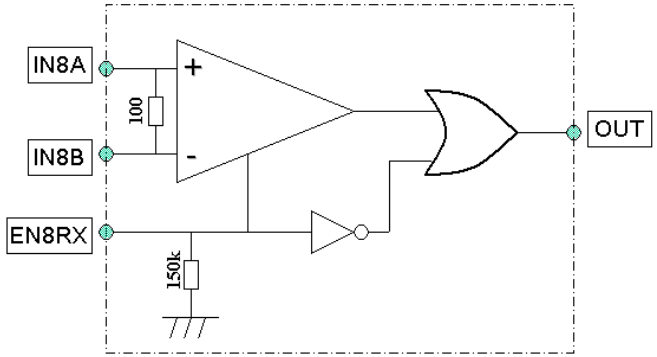
LVDS_RX Datasheet summary

- Logic diagram



Channels 1to 7 of CMS-ECAL LVDS_RX Receiver

Specific design for the eighth channel



Channel 8 of CMS-ECAL LVDS_RX Receiver

Function Table channels 1 to 7

DIFFERENTIAL INPUT Vdiff=V(INA-INB)	OUTPUT
Vdiff ≥100mV	H
-100mV< Vdiff <100mV	Undefined
Vdiff ≤ -100mV	L

Function Table channel 8

EN8RX	DIFFERENTIAL INPUT Vdiff=V(IN8A-IN8B)	OUT8
L	Don't care	H
H	Vdiff ≥100mV	H
H	-100mV< Vdiff <100mV	Undefined
H	Vdiff ≤ -100mV	L

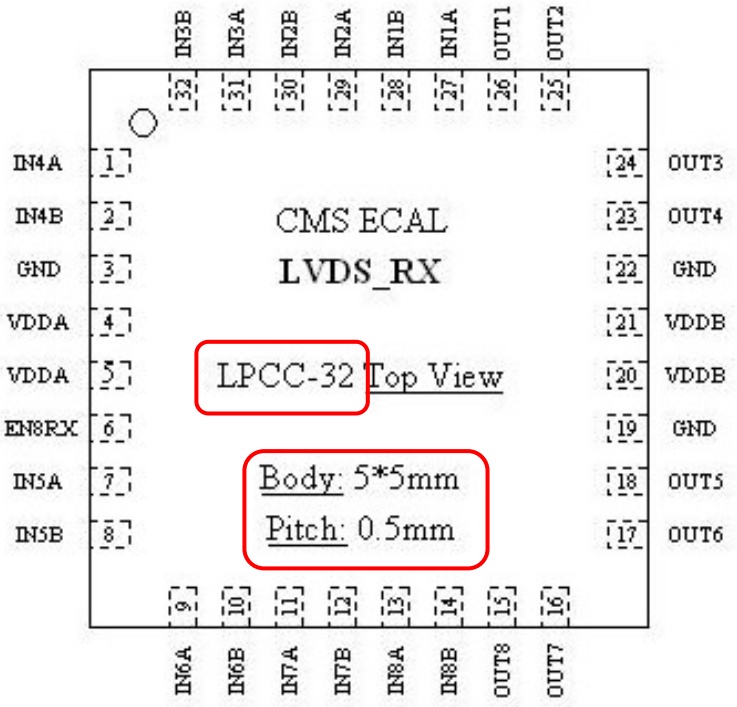
Sleep mode = no DC current

Datasheet (cont.)

• Performances

- Vdd: 2.5V
- DC current: < 21mA (7 active channels)
  (library LVDS cell slightly modified)
- Propagation delay < 6ns
- Output signal rise & fall time ~2ns
- Power consumption @40MHz: 100mW

• Package

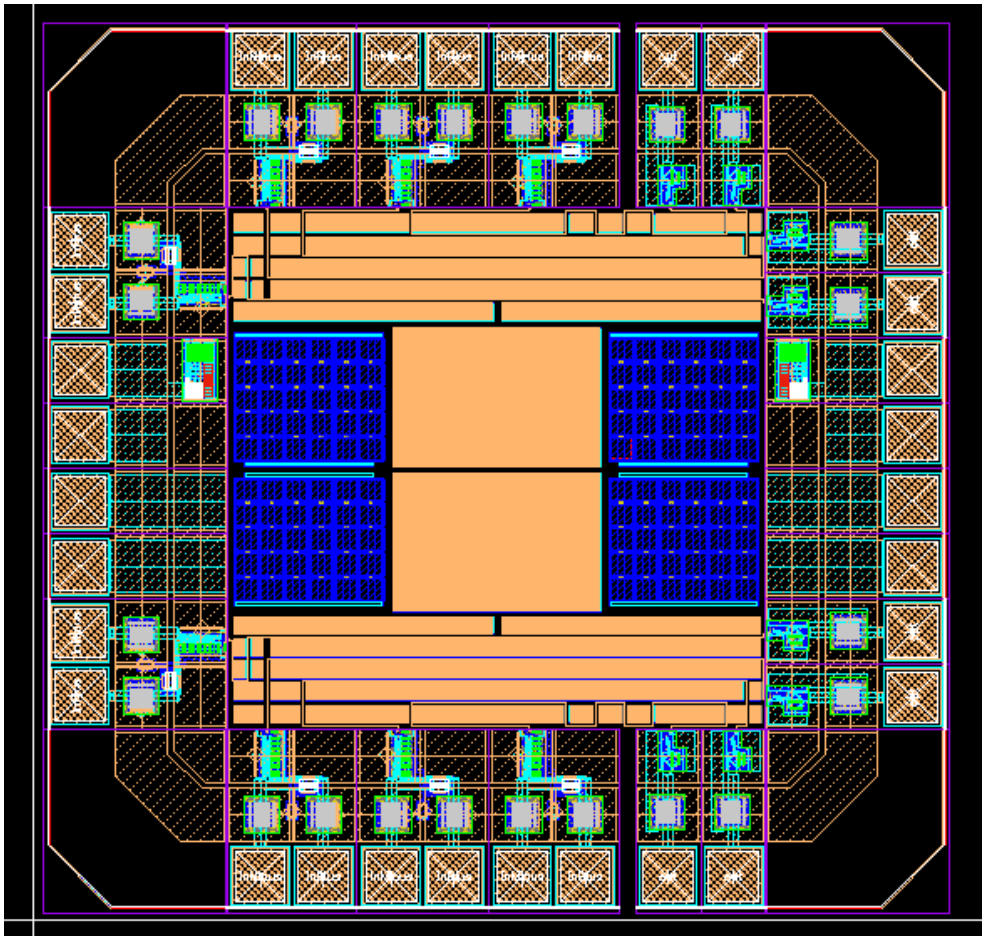


• Product identifiers

LYON CRT910 2004

LVDS_RX Layout

- Surface: 2mm*2mm
- Fonderie Altis 03/04



LVDS_RX Testing company choice

- Microtec has probably much more test experience than Edgetek

Nevertheless

- Testing the LVDS_RX chip is not a hard task

Edgetek :

- Owns up to date Automated Test Equipement for high volume production
- Has given a competitive budgetary quotation
- Wants to show that he is capable

In Conclusion

We:

- Think that Edgetek deserves to get our confidence
- Would suggest to give to Edgetek the LVDS_RX production tests

LVDS_RX: la note ! (1/2)

LVDS_RX SILICON COSTS	
DIE SIZE	2mm * 2mm
NB OF working LVDS_RX NEEDED	200K
NB OF INSTANCIATIONS IN RETICLE	38
NB OF RETICLE PER WAFER	105
NB OF LVDS_RX PER WAFER	3990
WAFER OCCUPANCY RATIO (LVDS_RX area/ reticle area)	51%
Recall: ENG RUN NB OF WAFER	6
Recall: PROD LOT NB OF WAFER AVAILABLE	48
Recall: ENG RUN COST	$130 000
Recall: 1 PROD LOT COST	$100 000
NB OF LVDS_RX DELIVERED (ENG RUN)	23940
NB OF LVDS_RX DELIVERED (1 PROD LOT)	191520
TOTAL NB OF LVDS_RX DELIVERED (ENG RUN + 1 PROD LOT)	215460
LVDS_RX ENG RUN OWN COST (differential costs return to CMS TRACKER)	$66 043
LVDS_RX PROD LOT OWN COST (differential costs return to CMS TRACKER)	$50 802
TOTAL LVDS_RX SILICON COSTS	$116 845

→ ~102 k€

LVDS_RX: la note ! (2/2)

BACK-END COSTS				
PACKAGING				
MANUFACTURER	ASAT			
PACKAGE TYPE	LPCC32			
NUMBER OF PACKAGED IC		200000		
UNIT PRICE ASSEMBLY COST (1)		$0,20		
TOTAL PACKAGING COSTS		$40 000		
TEST				
SUPPLIER	ASAT	MICRO-TEC	EDGETEK	HCM
LOCATION	Hong-Kong / ASIA	Stuttgart / GERMANY	Paris / France	La Rochelle / France
NRE COSTS		€ 25 800,00	€ 8 000,00	€ 4 966,00
ELAPSE TIME		6-7 Weeks	5-6 Weeks	7 Weeks
TEST PRICE PER COMPONENT (2s)		€ 0,09	€ 0,17	€ 0,40
TOTAL TEST COSTS		€ 43 800,00	€ 42 000,00	€ 84 966,00

→ ~35 k€

(1) Estimated price. Formally negociated with ASAT by A.Marchioro

Soit au total (Silicium + Packaging + Test) ~ 180 k€

LVDS_RX Time Schedules

- Engineering run chips currently at ASAT for assembly
- Purchassing order with the testing company ➔ May 11th
- Production test set-up ready ➔ June 20th

  (remark: ATE test socket making need 5-6 weeks)
- Lab Test board under development (few samples characterisition)

  Forecasted availability ➔ June 10th
- Production run launch forecast ➔ early in July