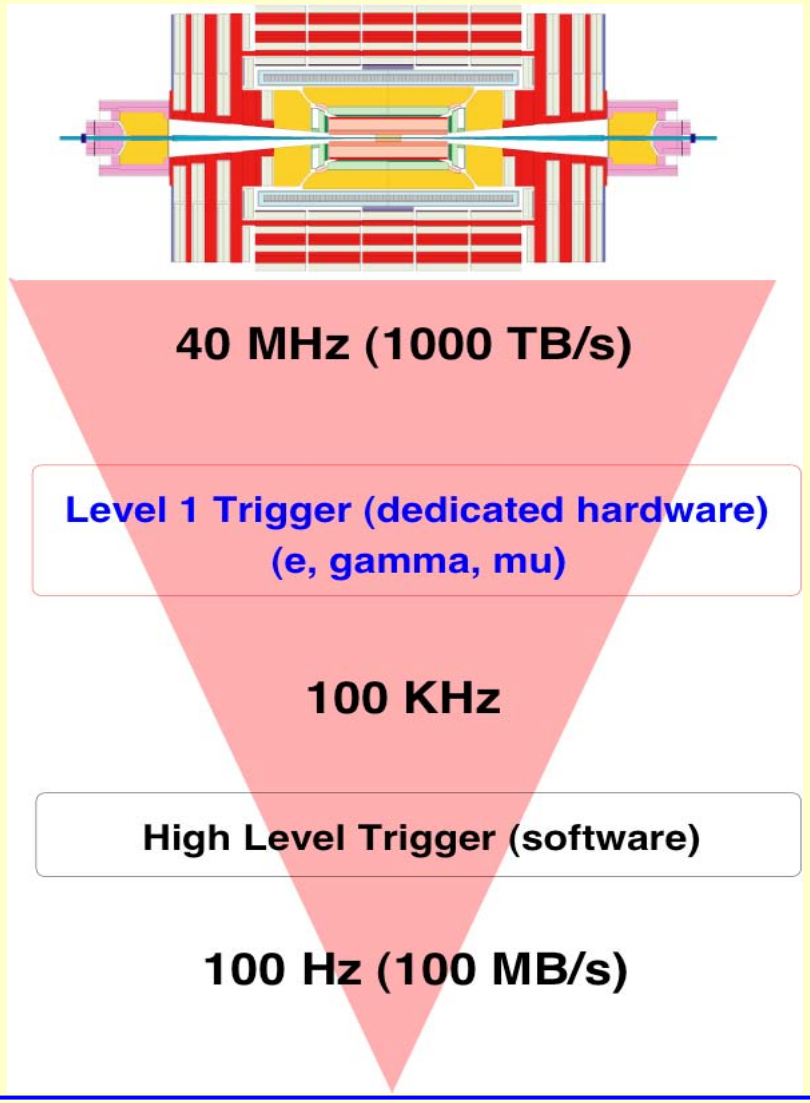
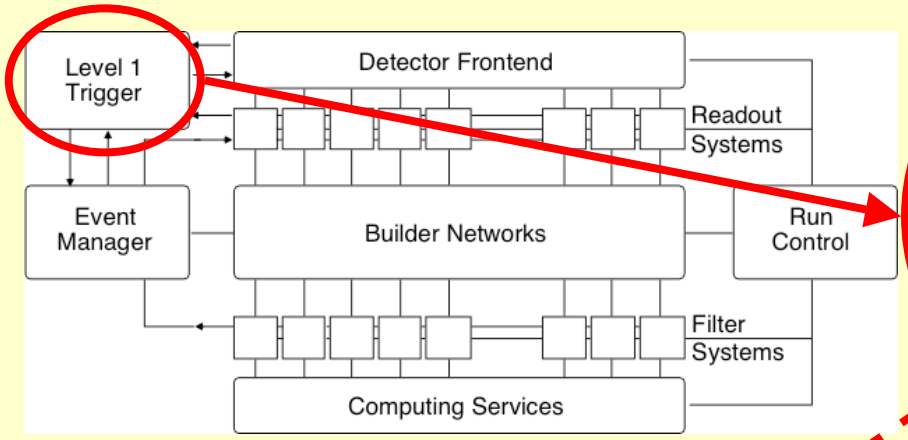
La génération des primitives de Trigger du ECAL

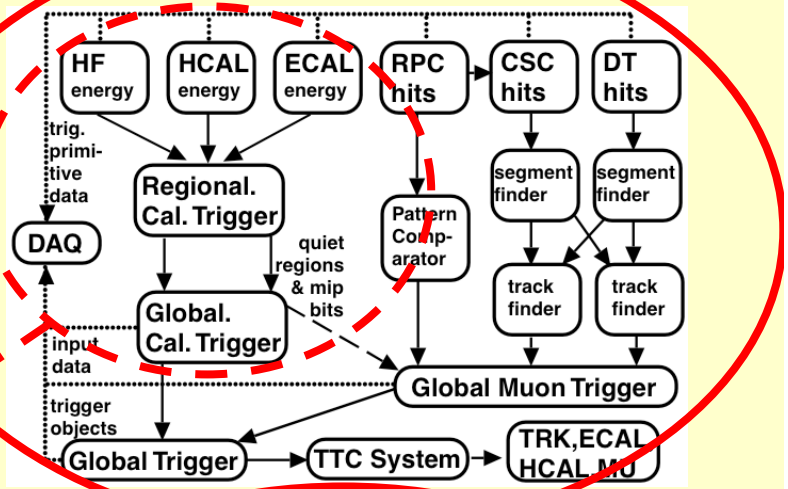
Le trigger c'est quoi?

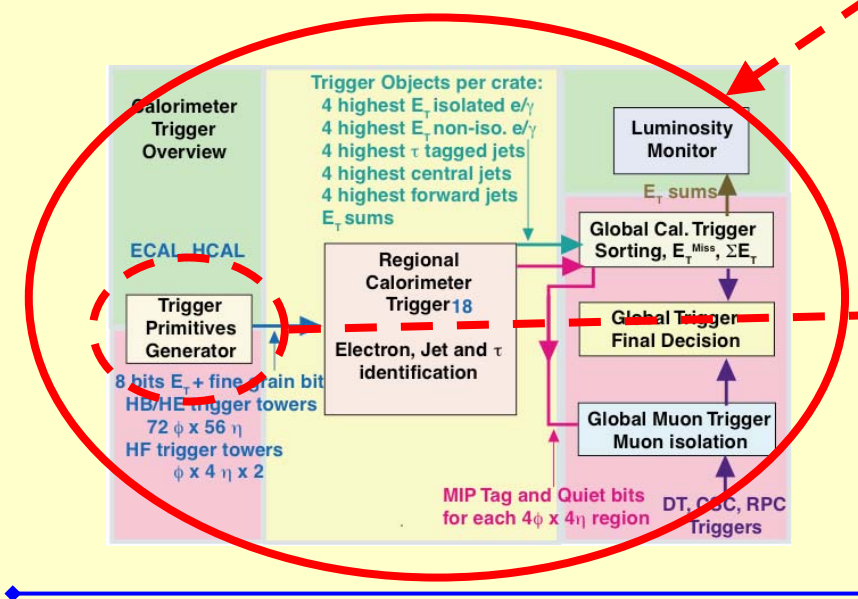


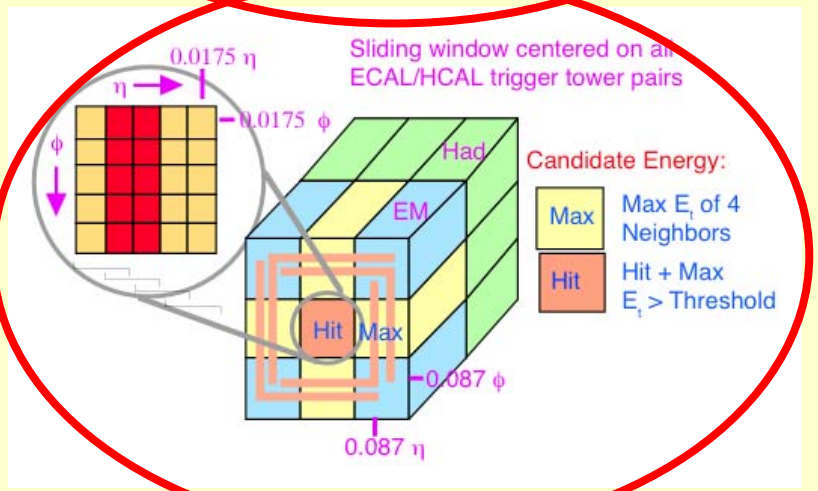
Les TPG c'est là !

Les TPG c'est quoi ?



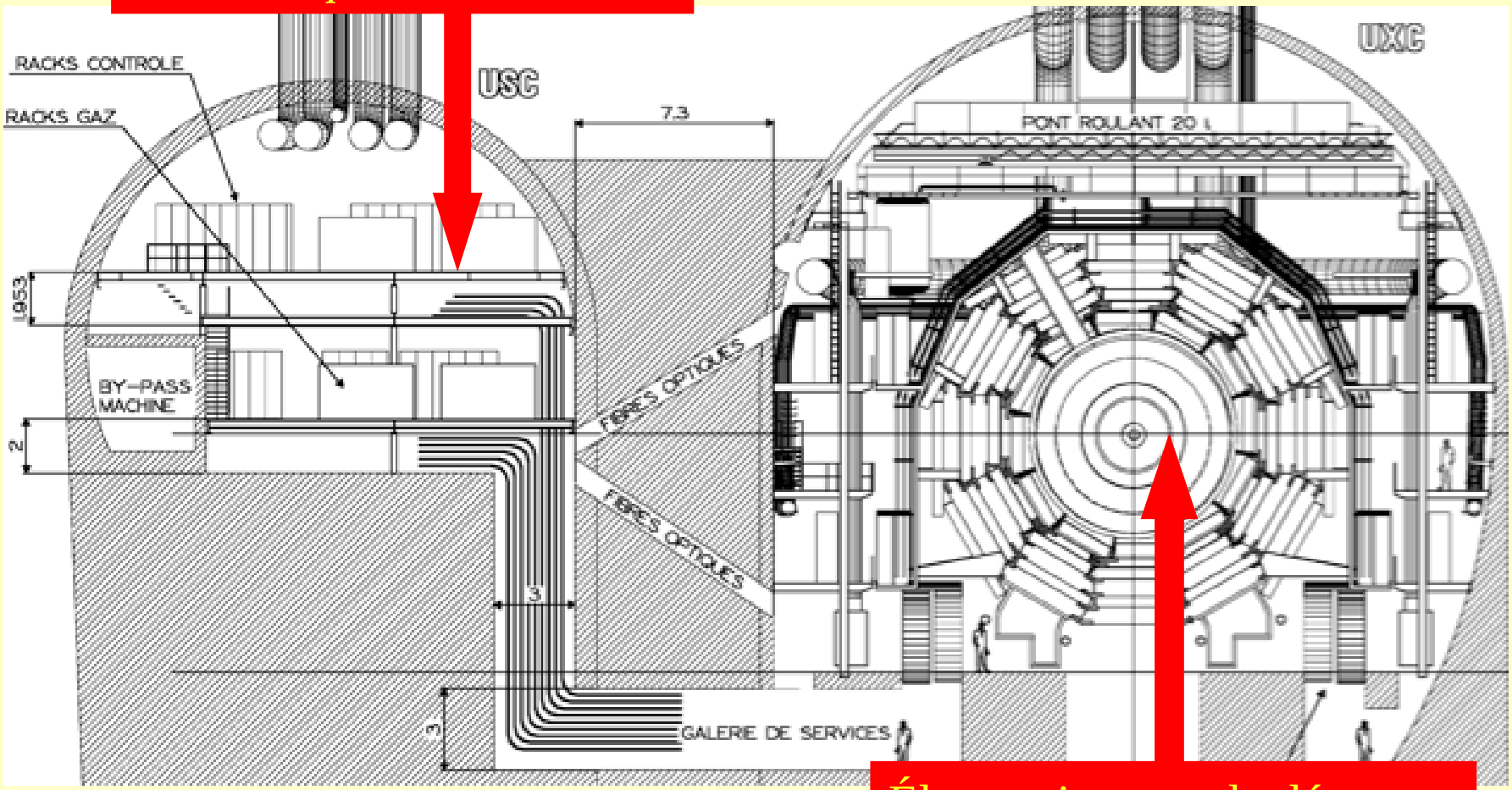






Les TPG c'est où ?

Électronique hors détecteur



Électronique sur le détecteur

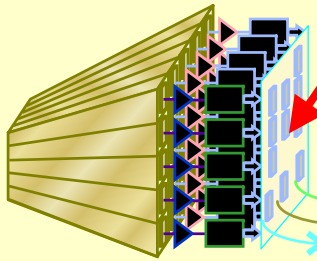
The ECAL Trigger Primitives Path

On Detector electronics

FE board:
- FENIX Strip
- FENIX TCP

Off Detector electronics

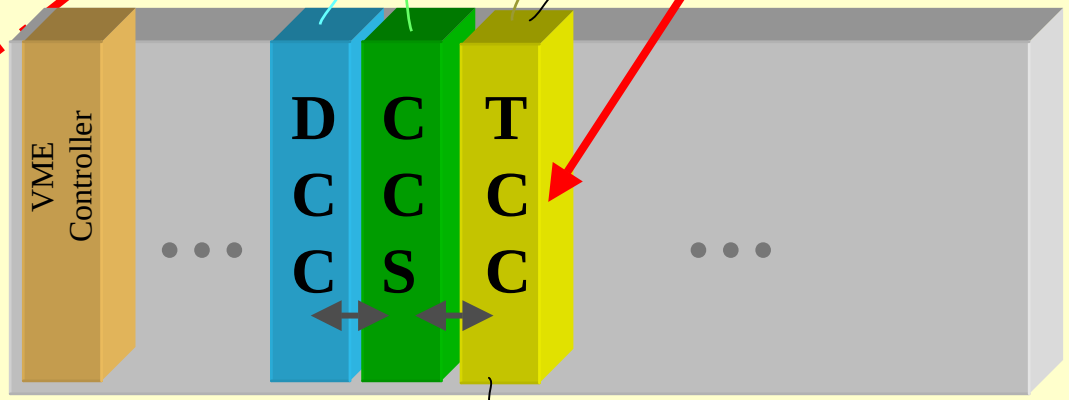
- Trigger Concentrator Card
- Synchro&Link Board



Timing, Control & L1A

Trigger primitives

Xtal Data



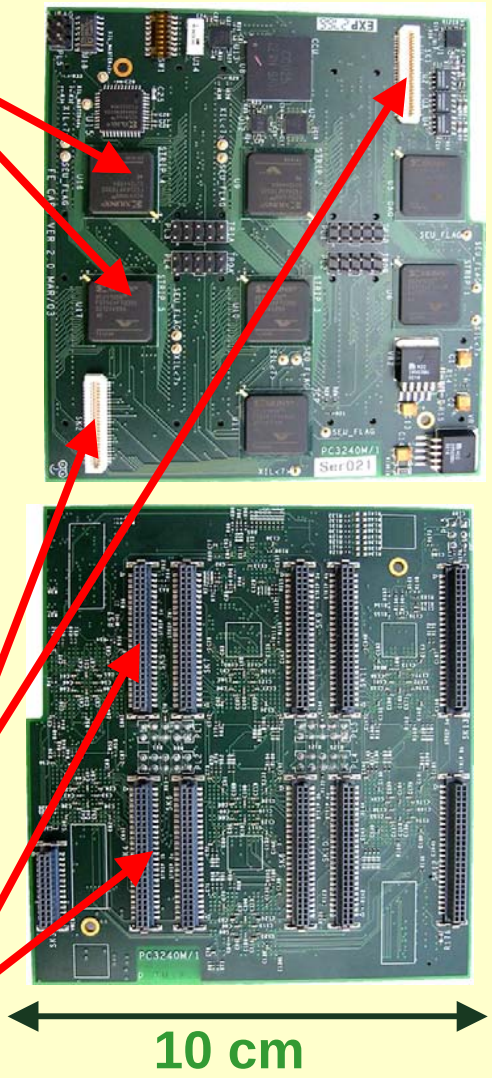
To SRP

To RT

Et maintenant… la Carte Front End

- La carte FE:
  - reçoit le signal d'une tour trigger (25 cristaux des VFE)
  - stocke les données dans l'attente d'un signal L1
  - Calcule les "Trigger Primitive"
  - formate et envoie les data (via GOL) vers le DAQ (carte DCC) à la réception d'un signal L1
  - envoie les "Trigger Primitive" à la carte TCC @40 MHz (via GOL)

Voir talk d'Akli Karar

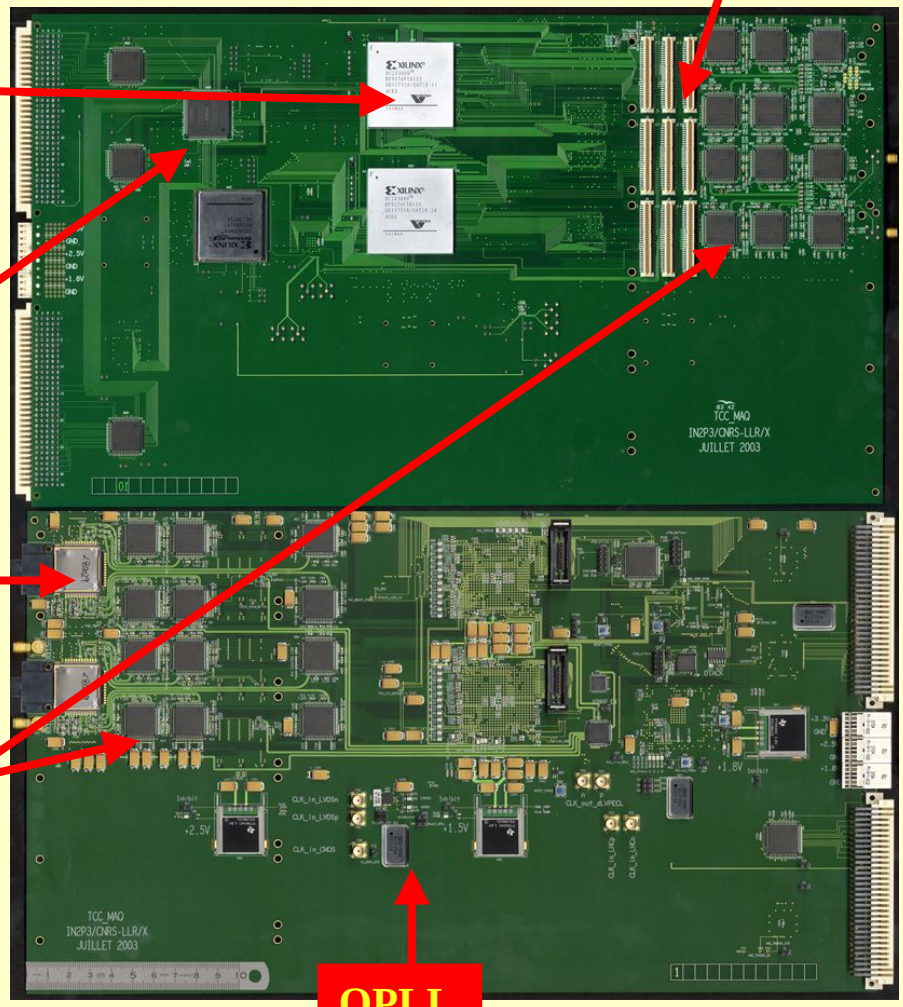


Et … la Trigger Concentrator Card (TCC)

Carte TCC :

1. Finalise les Trigger Primitive en provenance du Front End (encodage + composition tours trigger pour endcap)
2. Transmet les Trigger Primitive au trigger régionale @40 MHz et à la carte DCC (vers DAQ) @L1

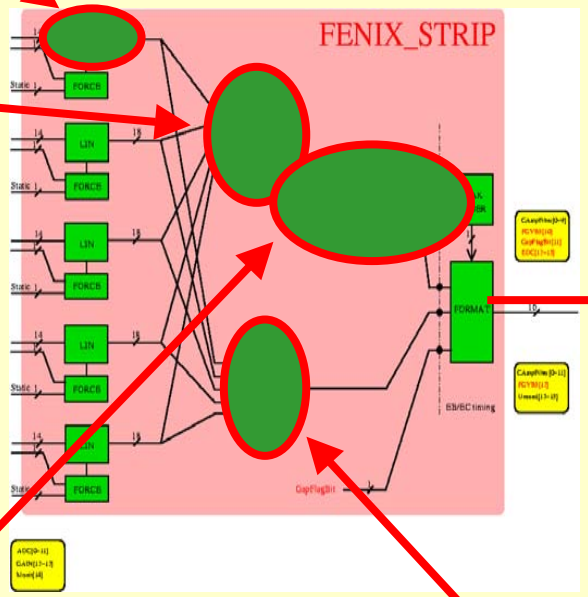
Voir talk de Yannick Geerebaert

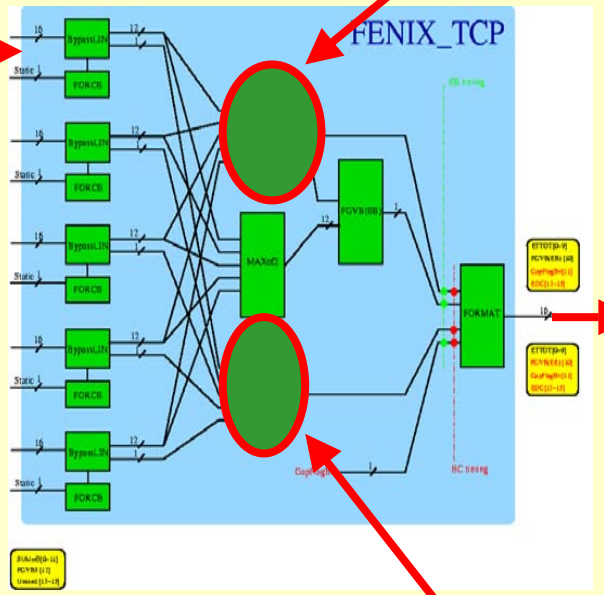


Zoom sur les TPG coté Front-End

linearization
from 12+2 to 18

strip or
pseudo
strip
signal





total E_T

TCC

BCID FIR filter +
Peak Finder

Fine Grain
Veto Bit

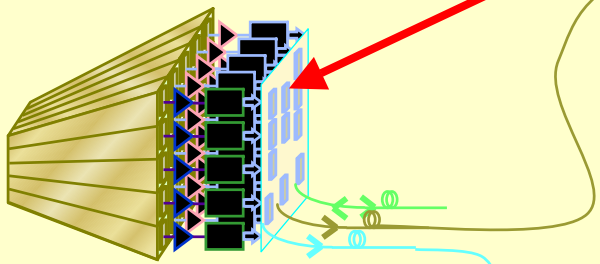
Fine Grain
Veto Bit

Validation des TPG

(Cf Nicolas Regnault, calor2004)

H4 test beam set-up:
- FPPA

FE board:
- FPGA FENIX Strip
- FPGA FENIX TCP



30 samples of Recorded TP

30 samples of SystemC TP

continuous output stream of SystemC TP

continuous output stream of ASIC TP

System C simulation (LLR)

25 X 14 samples of Recorded Crystal Data

Continuous input stream (LLR)

ASIC simulation (RAL)

SystemC : le VHDL du physicien…

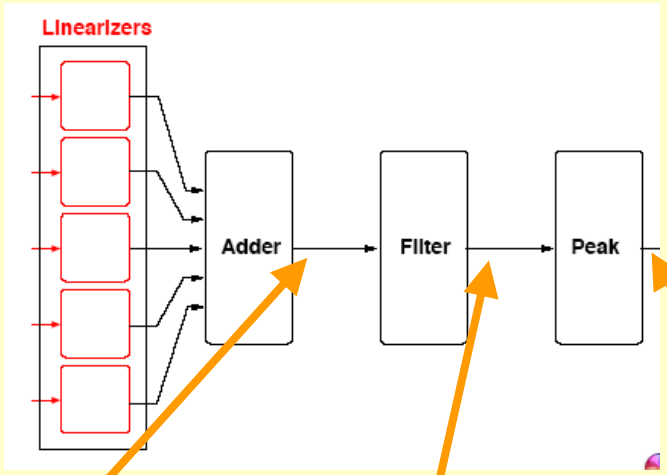
- Framework de simulation et de design d'électronique numérique (C++)

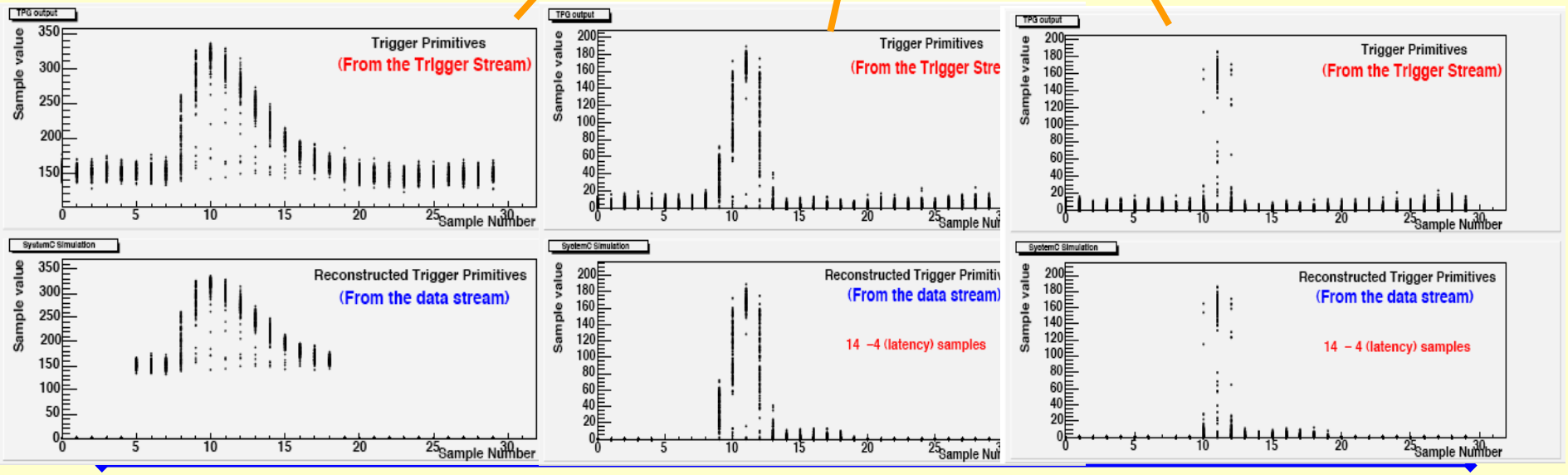
- Gratuit, Sources disponibles, GNU software (http://www.systemc.org)

- Mêmes fonctions que VHDL:
  - ports, signaux, process etc…
  - scheduler, moteur de simulation

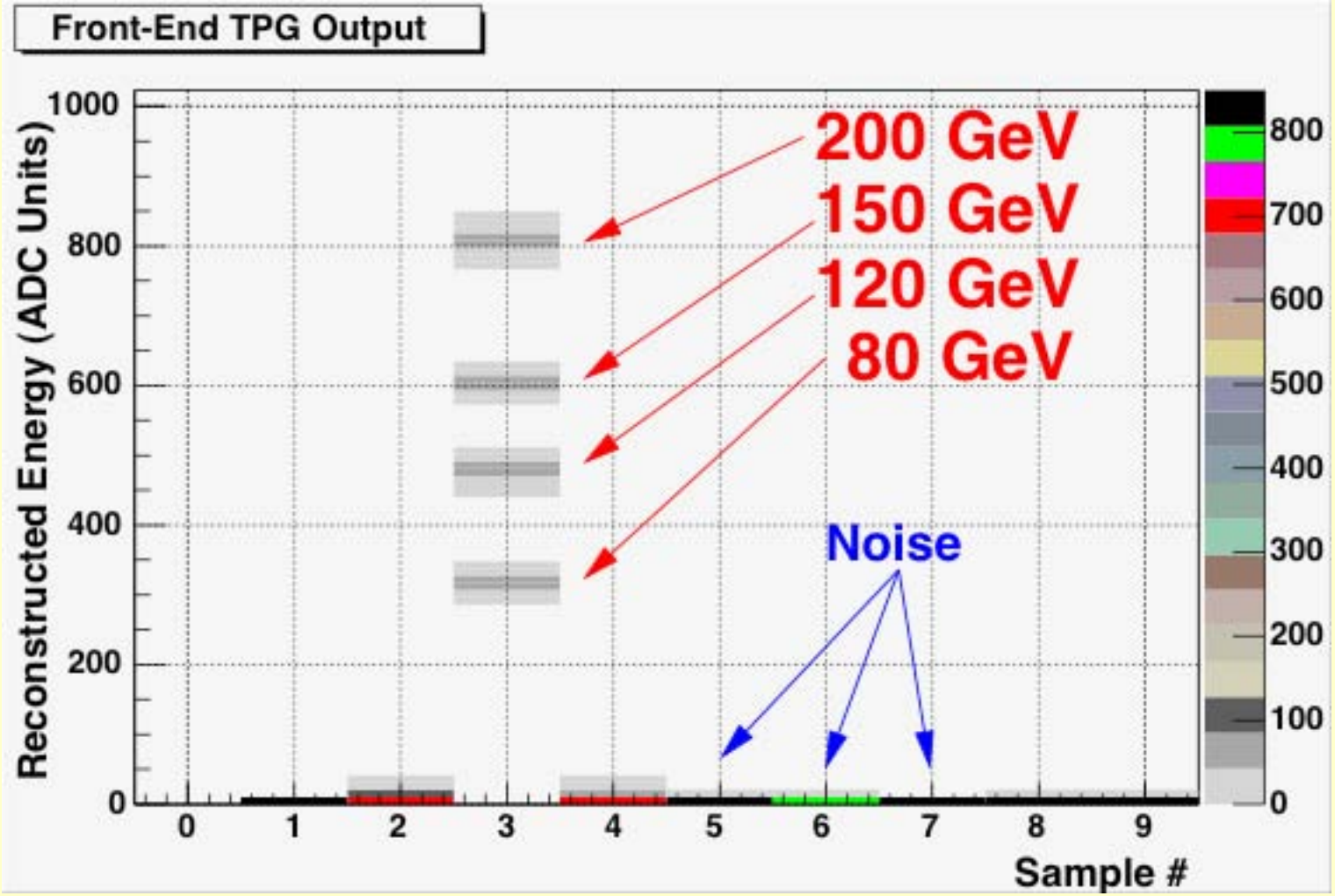
- Simple d'utilisation pour le physicien moyen… (c++)

Comparaison data/simulation

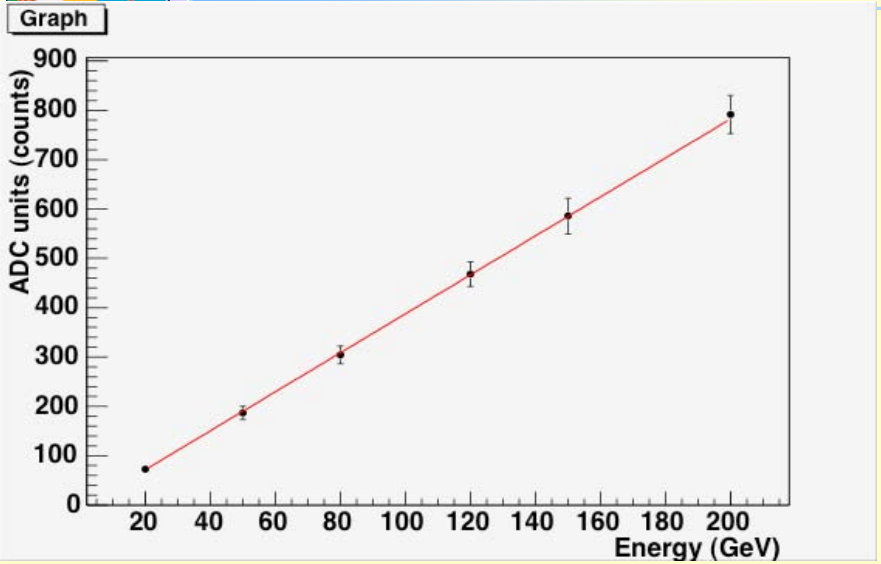




Reconstructed TPG output

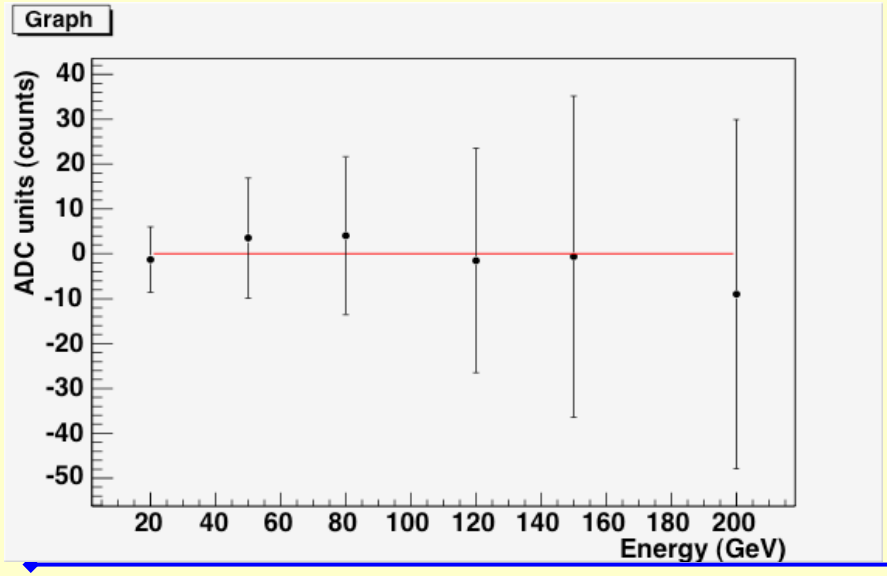


FENIX: TP linearity



Linearity of the TPG is excellent for energy in the [20,200] GeV range

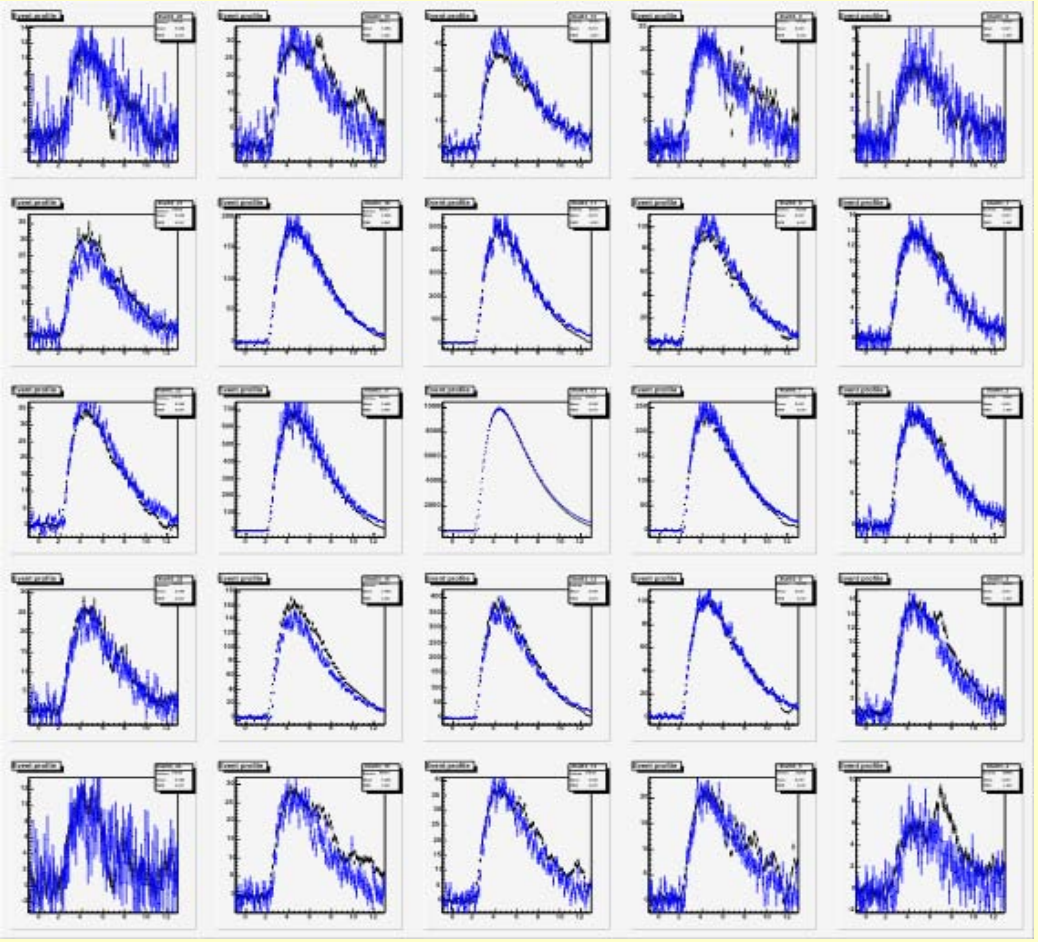
Energy = 0.25 ADC units



The bar length gives the RMS of the residues distribution

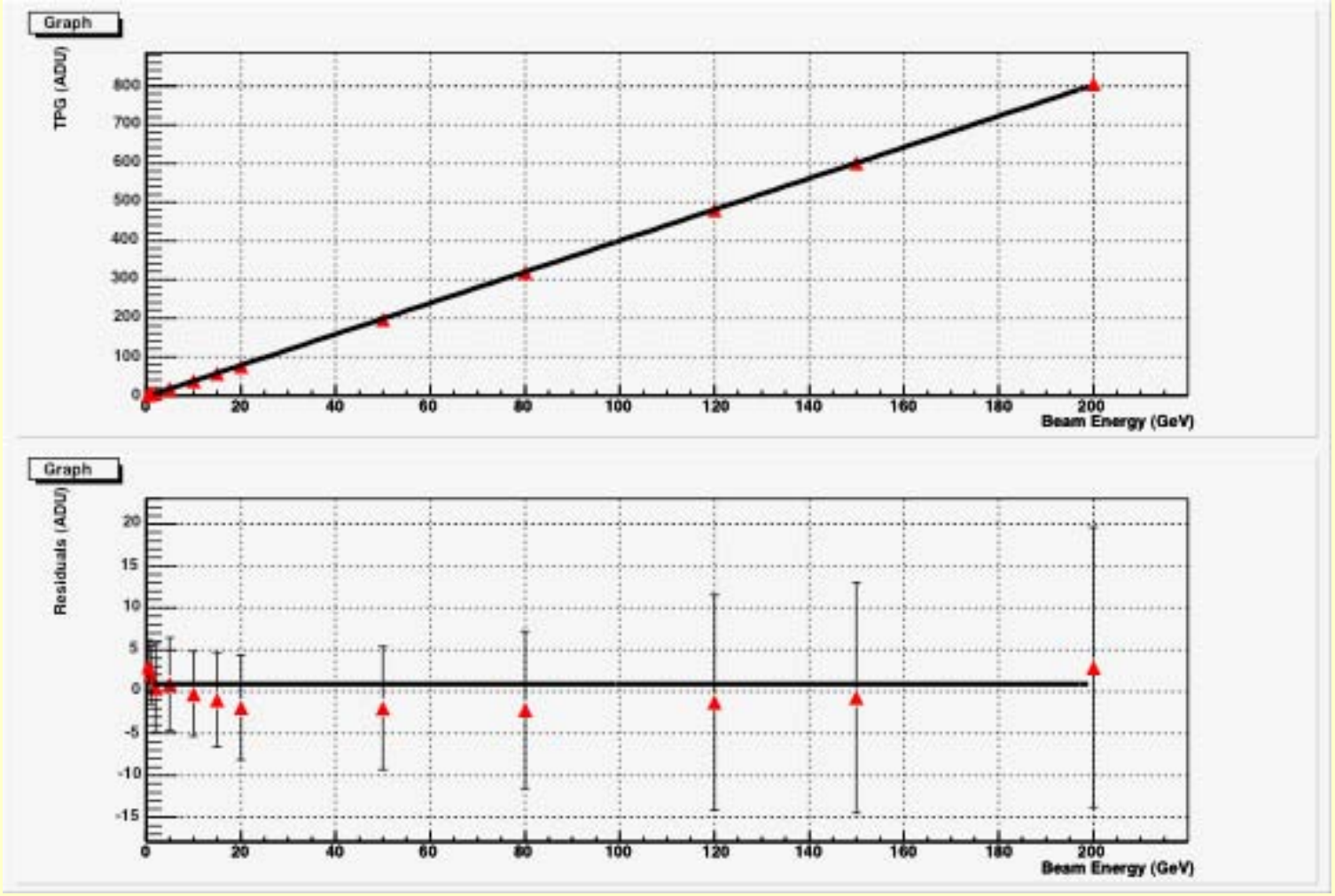
Studying the TP at low energy

⇒ **Need simulation:** no test beam data for energy < 20 GeV

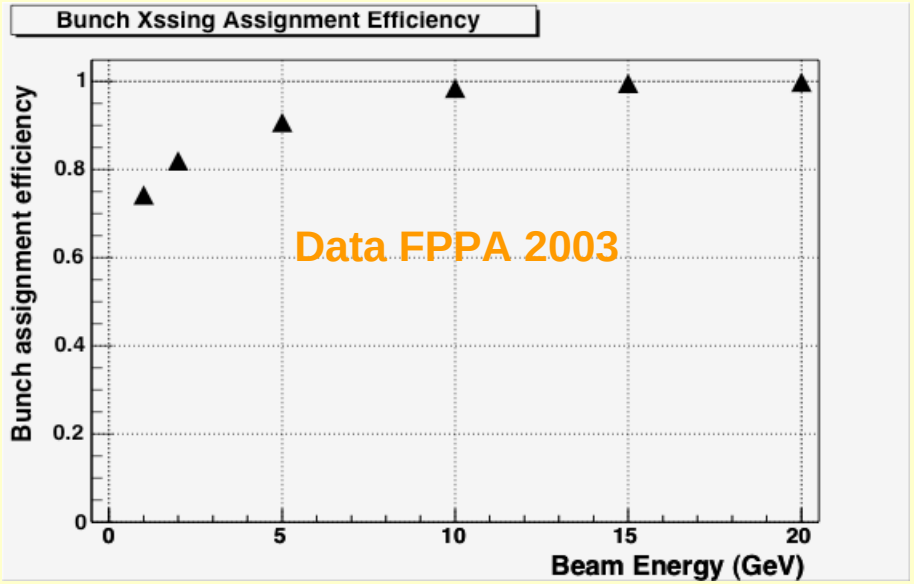


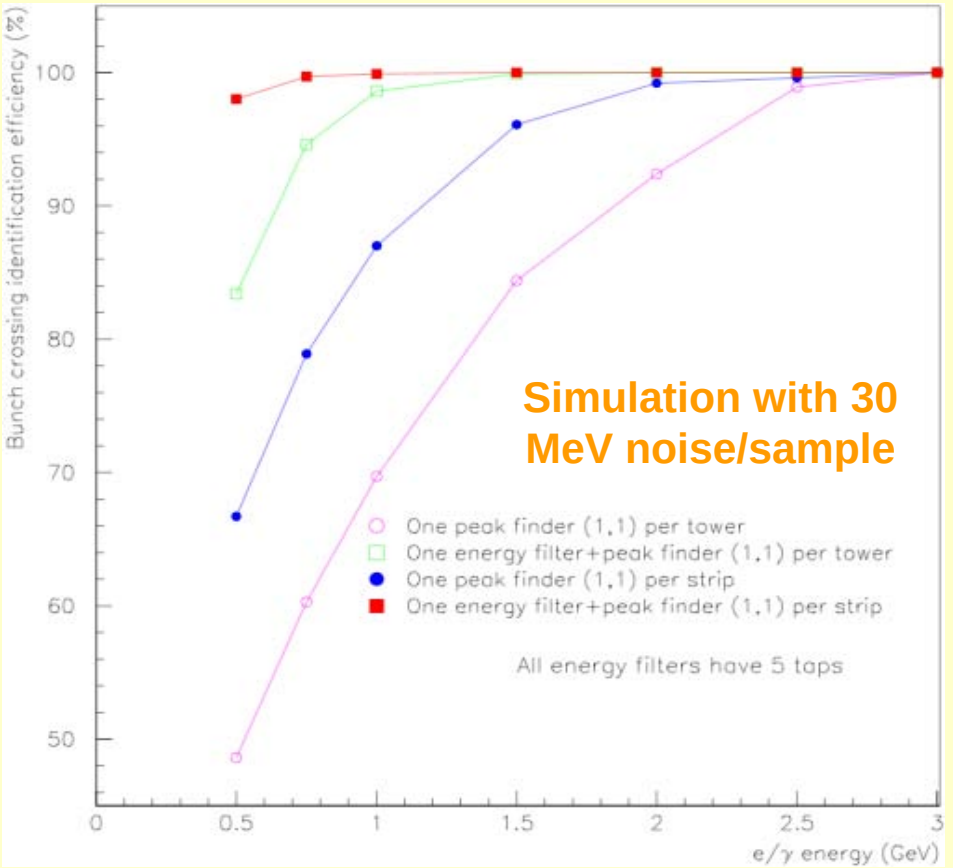
Extrapolation à basse energie: simulation GEANT4 du test beam h4sim+h4ana (Cf talk S. Bimbot)

TP Linearity



Bunch-crossing identification





Bunch Crossing ID is excellent for energy > 10 GeV

Hope to improve Bunch Crossing ID for lower energy (better shielding in the final version of the VFE)

⇒ MGPA analysis in progress

Detecting low energies (≈ 0.5 GeV) is mandatory for:

- **ECAL isolation energy around em cluster criterium**
- **good operation of the synchronisation of the ECAL TP**

Conclusion

- **Les TPG ont été testées pour la 1ere fois en condition réelle en 2003 en test beam.**

- **Une simulation détaillée du hardware a été réalisée (voie trigger des cartes FE)**

- **Avec cette simulation, les données testbeam et h4sim, la qualité des TPG a pu être étudiée jusqu'aux basses énergies**