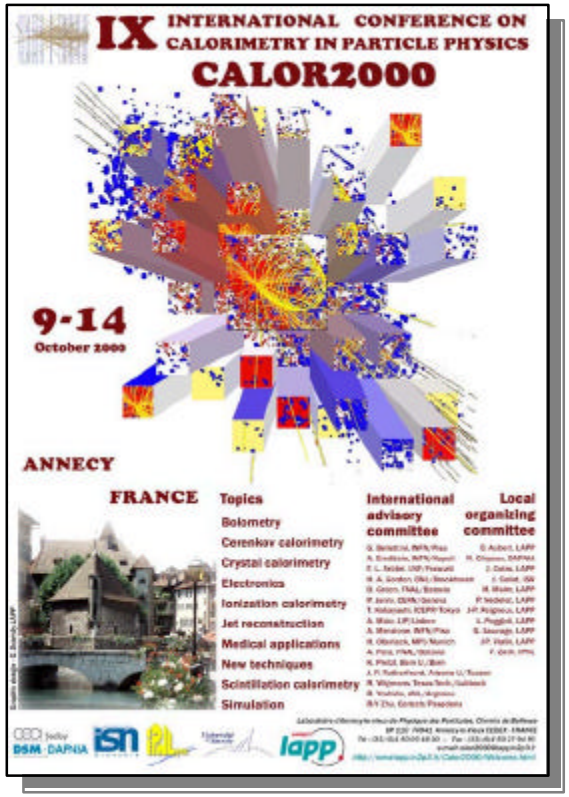
The Read-Out Driver (ROD) for the ATLAS Liquid Argon Calorimeters



Outline

- The read-out architecture
- The front-end boards
- The front-end links
- The read-out driver (ROD) modules
  - design considerations
  - prototype design and performance
  - next steps
- Summary

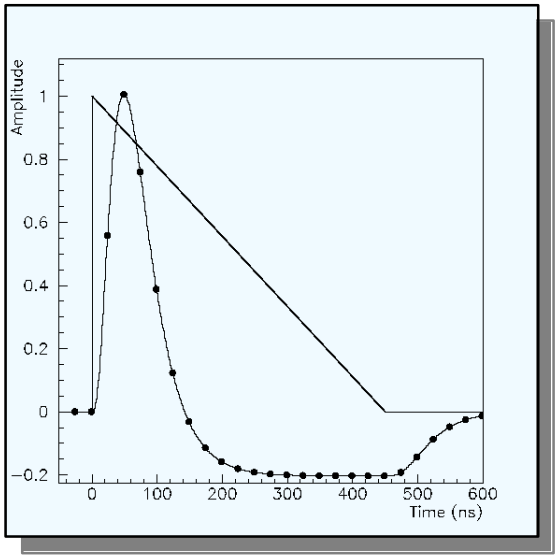
Ilias Efthymiopoulos, University of Geneva

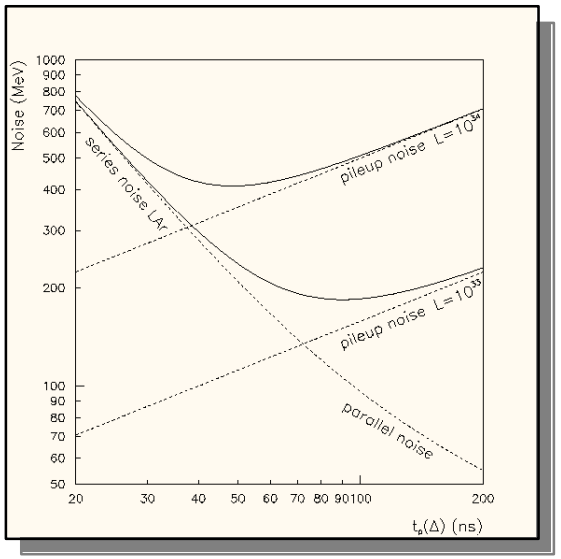
Calor 2000, Annecy October 10, 2000

The LArgon read-out architecture

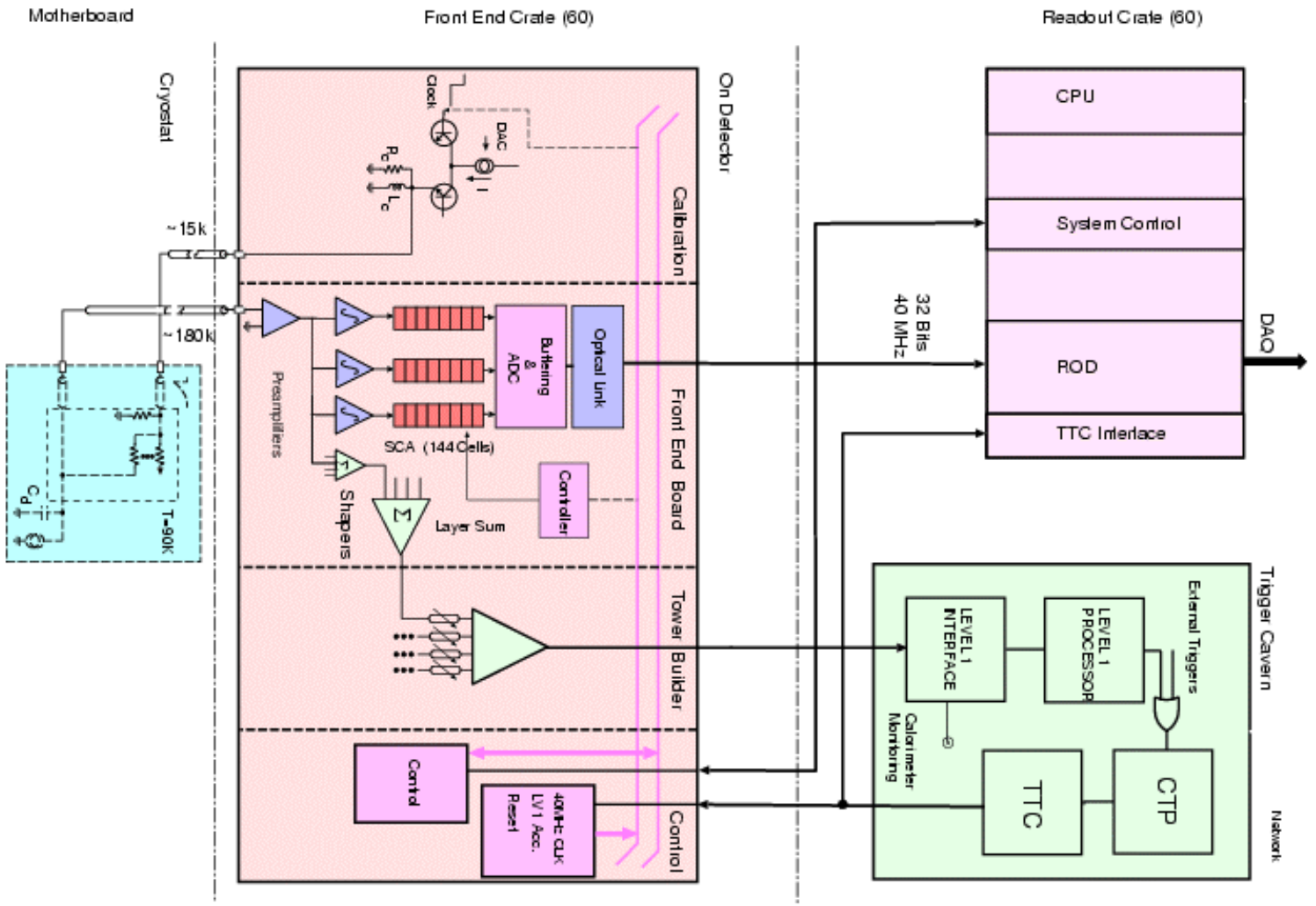
Design considerations

- minimal signal degradation due to the read-out chain
- data send to both Lvl1 & DAQ
- large dynamic range:
  - em:
    - up to ~3TeV (10mA)
    - irreducible pile-up noise ~50MeV
    - 16-bit dynamic range
  - hec: up to ~1TeV (0.3mA)
- calibration to 0.25%
- minimal coherent pick-up noise
- fast shaping to optimize signal/noise ratio
  - 40MHz sampling rate
  - digital filtering to adapt to changing machine condition
    - gain ×1.5 in noise at low luminosity
- minimal dead-time at 75KHz Lvl1 trigger rate
- radiation hardness:
  - 20Gy/yr; 10^{12} n/cm^2/yr

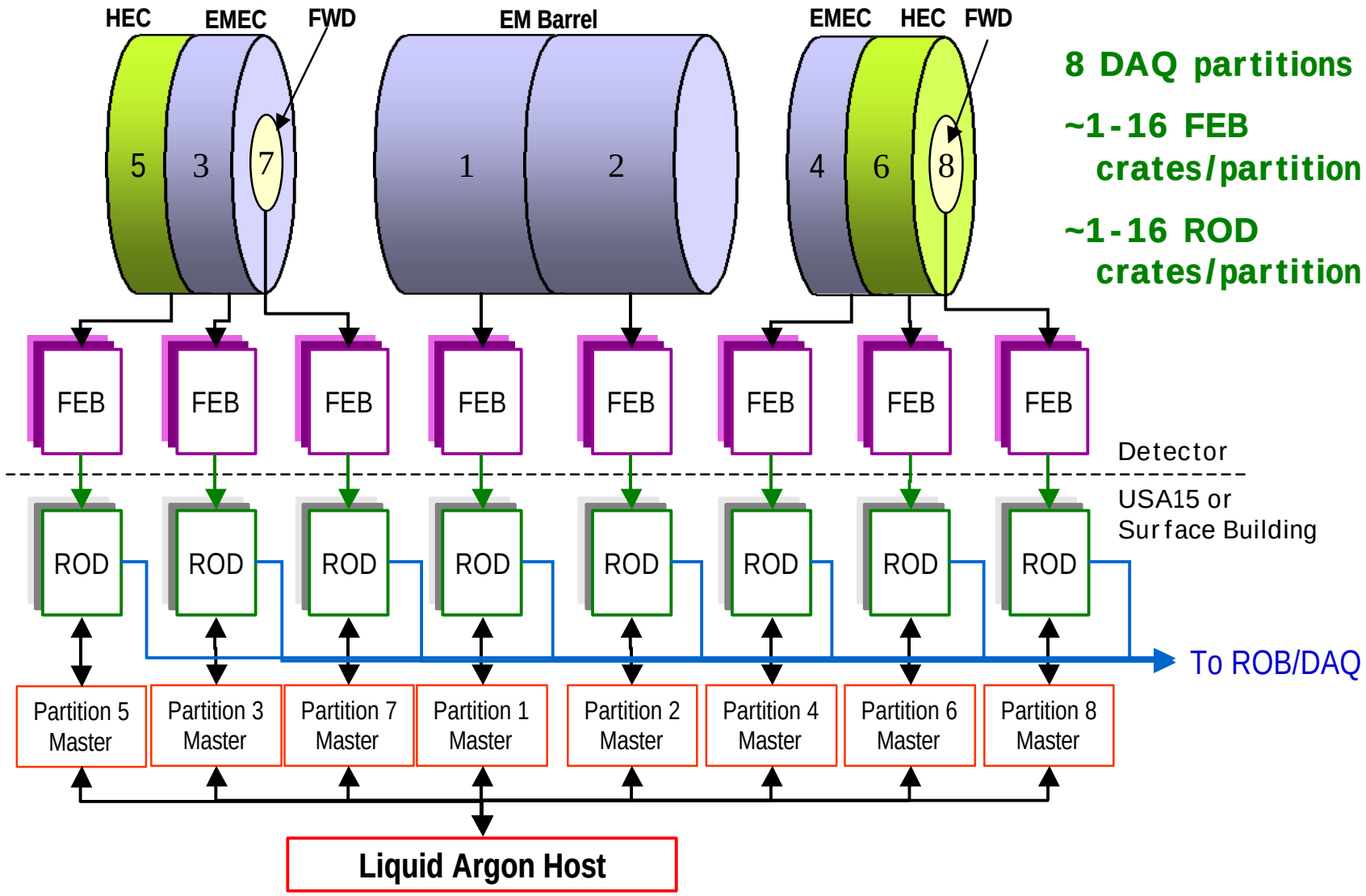




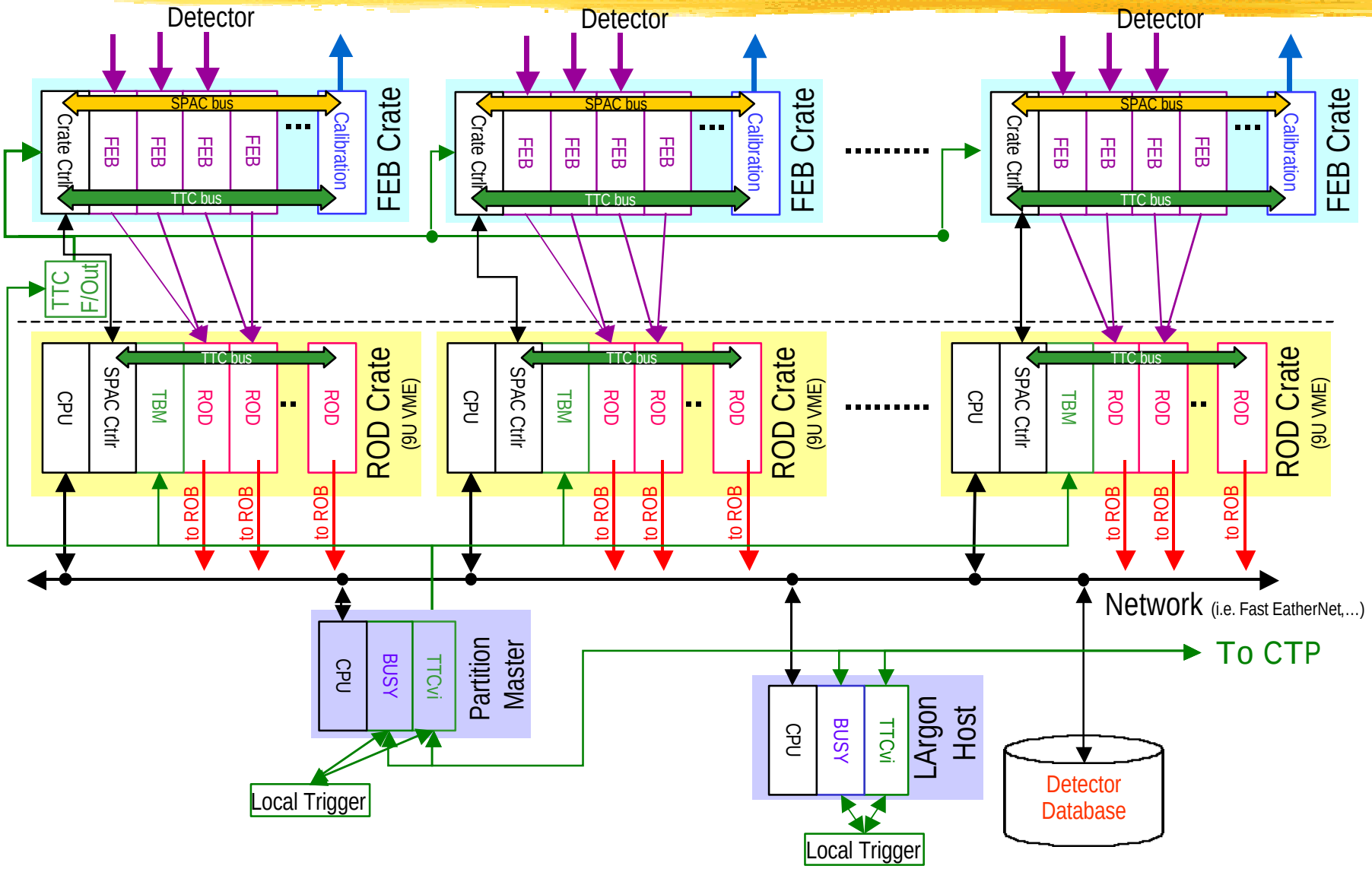
... The LArgon read-out architecture



... The LArgon read-out architecture



... The read-out architecture - Details of a partition



... The LArgon read-out architecture

Important system aspects

- very large system
  - ~190 000 channels
- front-end electronics
  - housed in crates (front-end crates)
    - attached to the cold to warm feedthroughs, in the crack between the barrel and end-cap calorimeters and at the rear of the end-caps
  - ~1700 FEB boards
    - 1 front-end link per board: 32bits@40MHz
  - 32 front-end crates (barrel), 2× 16 (end-caps)
- back-end electronics
  - baseline architecture (TDR)
    - 2 FEB boards (2×128ch) → 1 ROD board
  - ~54 ROD crates

The Front-end board (FEB)

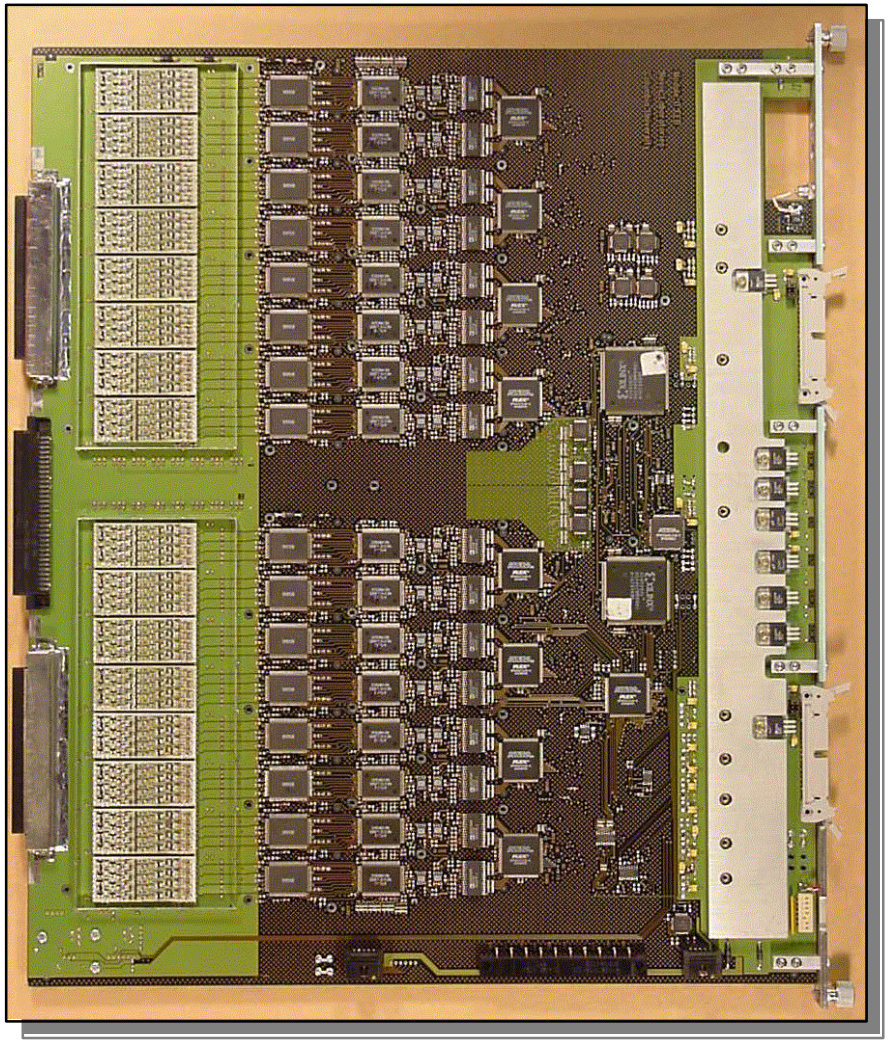
FEB architecture

board characteristics:

- 128ch/ 490×410mm² boards
- power consumption < 700mW/ch
- 16; 8ch (12-bit) ADC @ 5 MHz
- optical output of digitized data to the RODs (32-bit @ 40MHz)
- event-by-event gain selection for each channel based on peak sample

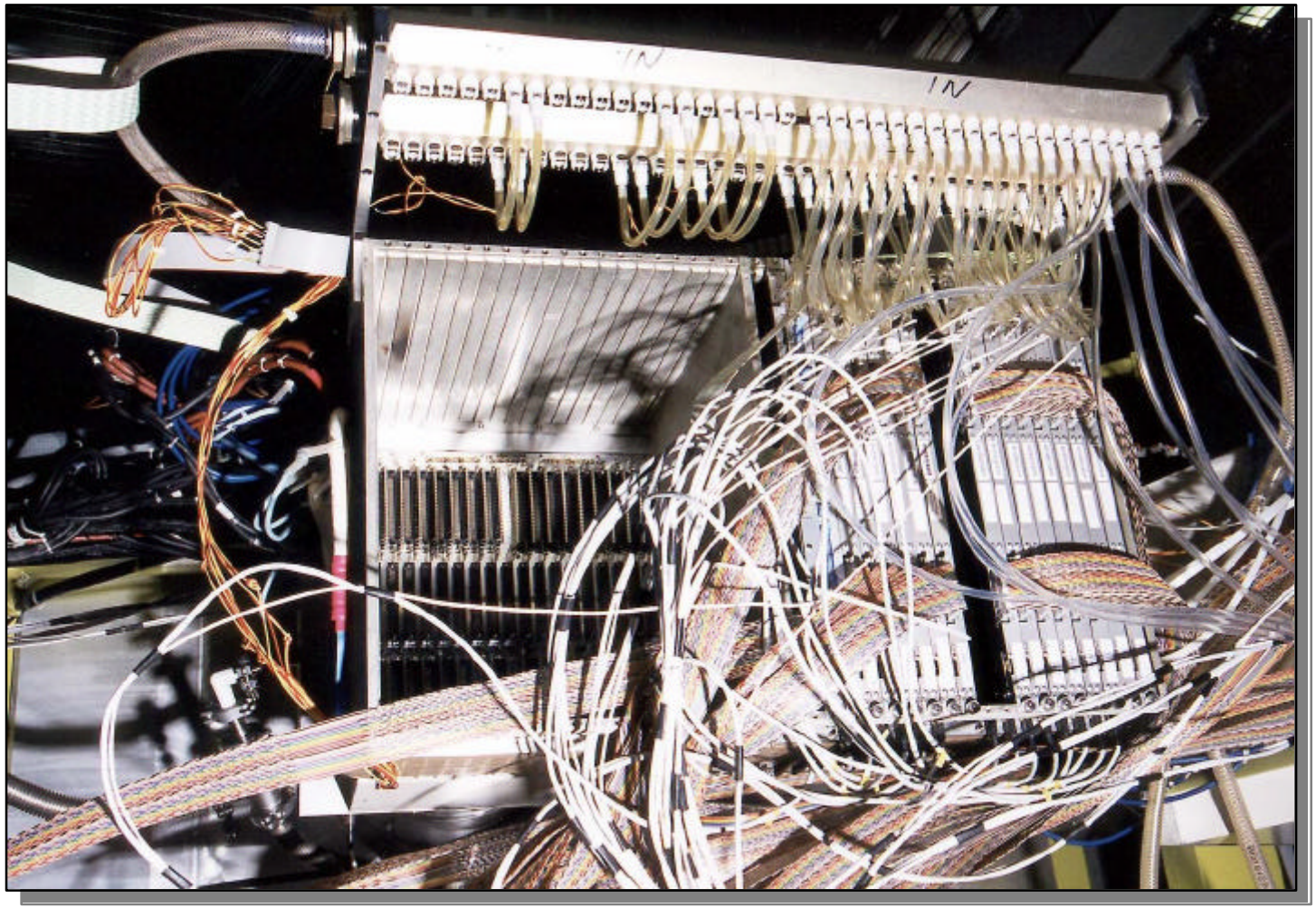
Collaborating institutes

Columbia University, LAL Orsay, CEA Saclay, Alberta, INFN Milano, BNL, Pittsburgh



... The FEB board

Front-end electronics crate at the test beam

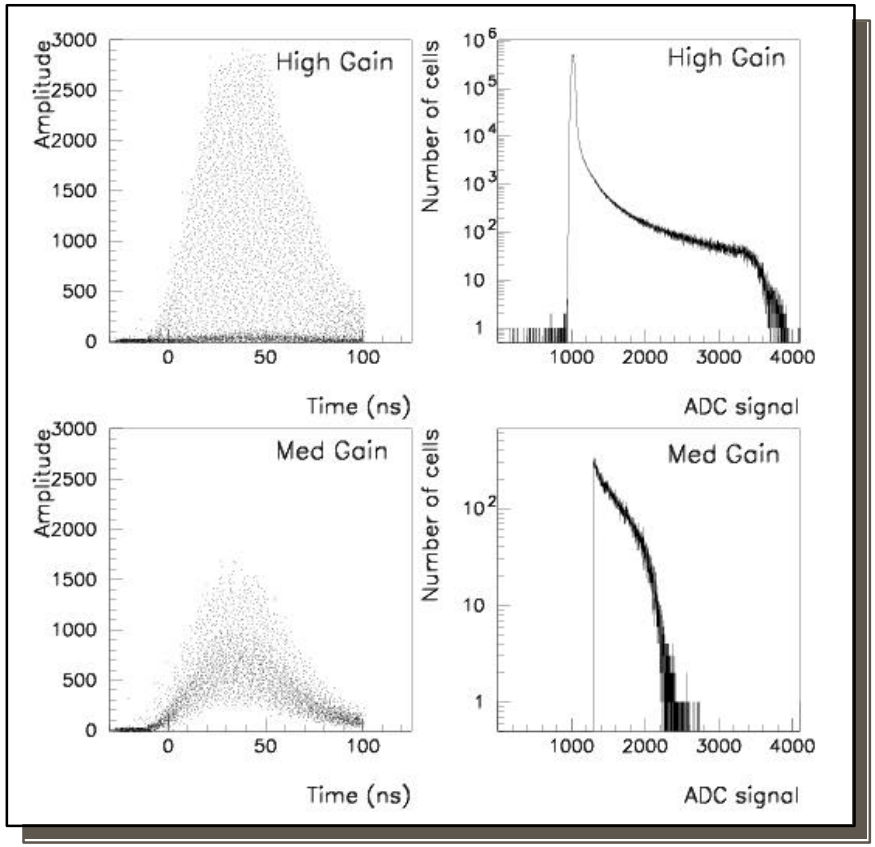


... The FEB board

Prototype FEB in test beam

hardware gain selection

- one threshold/FEB
  - ATLAS: one threshold/channel
- 3rd ADC sample on medium gain
- take into account:
  - pedestal dispersion
  - asynchronous beam
- no error in gain selection at 10^{-5} level
- noise (3×3 cluster)
  - fixed medium gain: 487MeV
  - free gain 300 MeV
- no difference in the energy resolution observed between free and fixed gain mode



... The FEB board

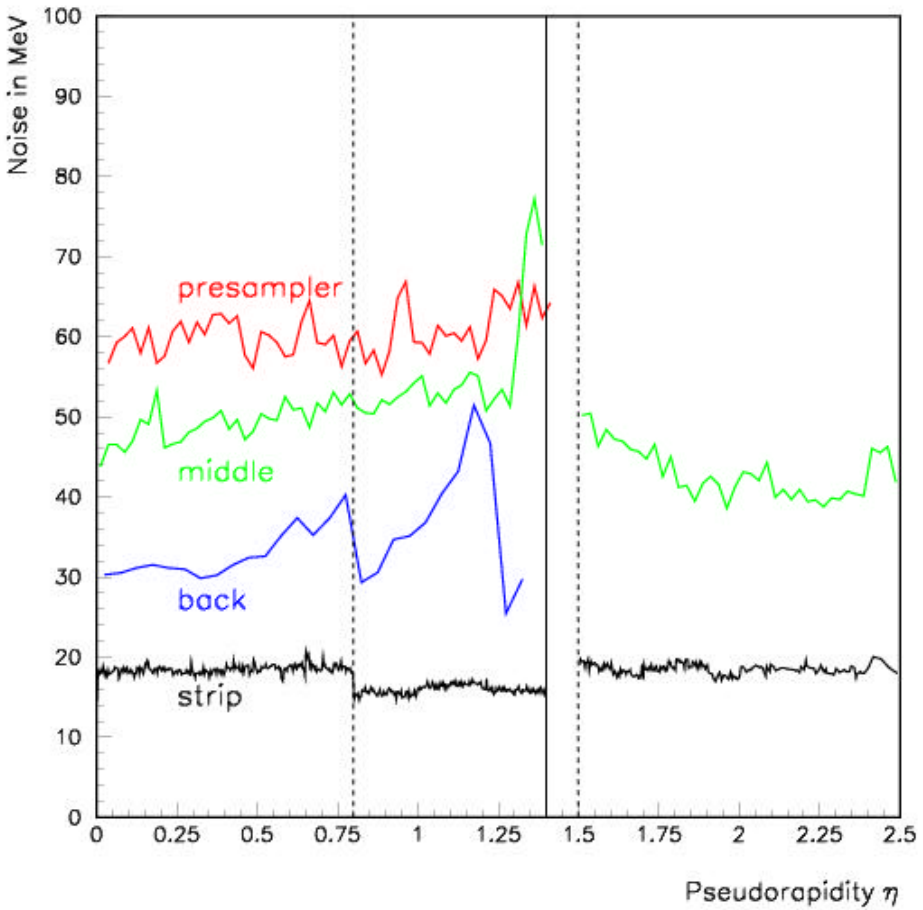
Prototype FEB in test beam

noise performance

- noise in ATLAS-like em cluster
  - covering 3×5 in middle layer
  - 278 MeV (251 incoherent noise)
- noise reduction with optimal filtering ~1.7
- gain uniformity/stability
  - gain dispersion in strips ~3%
  - gain stability <0.5%

more information in other presentations:

- **F. Lanni**, L.Kurchaninov (next...)
- **A.Kiryunin, C. Clement**, A. Minaenko, R. Orr (tomorrow)



... The FEB board

Status

- full size prototypes available
  - ~50 boards produced and tested in H8/H6 test beam
- final design validated in June '00
  - last element was the choice of the readout link technology
    - Sept '00 : Single G-link solution (see later)
- ongoing work for DMILL version
  - first chips expected before end '00
  - chip production should start by end '01
- FEB production readiness review (PRR) by May '02

The front-end links

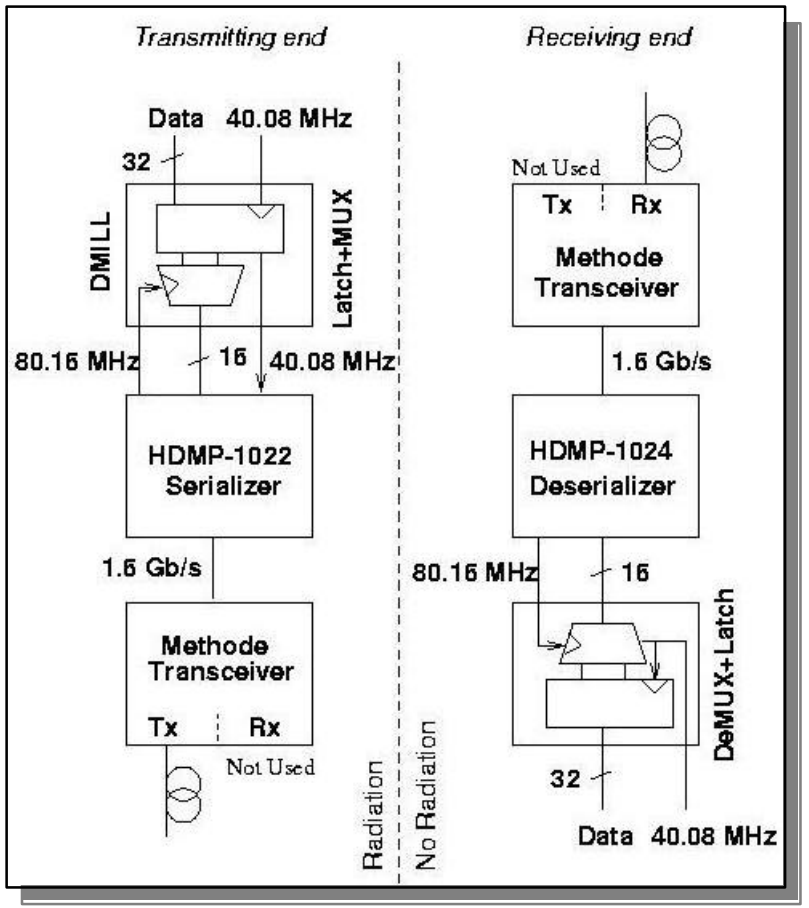
Design considerations

- Radiation tolerant optical links: 2 FEB's → 1 ROD
  - less material
  - high speed optical channel → less links (single fibre)
  - optically decoupled FEBs
  - less signal attenuation
  - less power dissipation
  - widely used → prices are dropping
- Several solutions studied
- Recently (Sep'00) the single G-link solution was adopted

Collaborating institutes

Academia Sinica Taiwan, CPPM, Marseille, ISN Grenoble, KTH Stockholm, SMU Dallas

single G-link block diagram

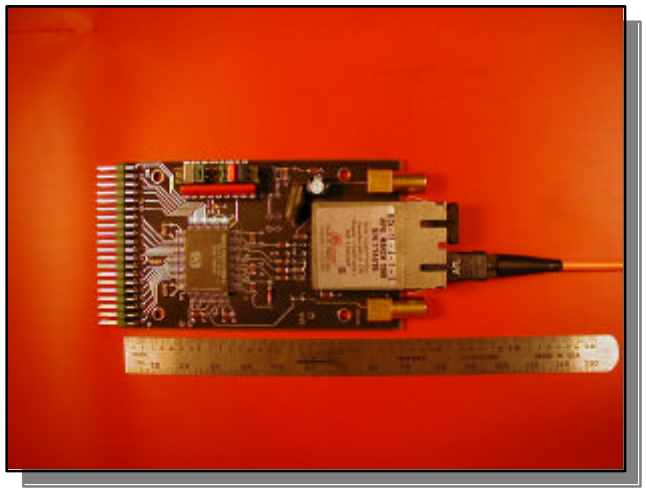


...The front-end links

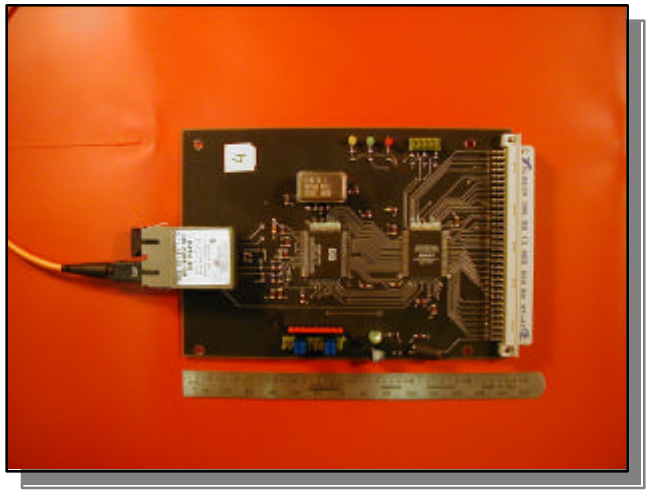
Single G-link

- long term tests in the lab (6 months); no errors observed
- BER < 10^{-16}
- power consumption:
  - Tx : 1.9W G-link, 2.7W total
  - Rx : 2.5W G-link, 4.1W total
- extensive radiation tests:
  - tests done at:
    - 3×10^{13} n (1MeV Si)/cm^2
    - 10 KGy (Si) of γ
  - errors observed:
    - single bit flips
    - frame or PLL loss
    - clock corruption
- with the error detection and/or correction available in the ROD the data losses in ATLAS will be minimal

- Tx board



- Rx board



The LArgon read-out driver (ROD) module

Design considerations

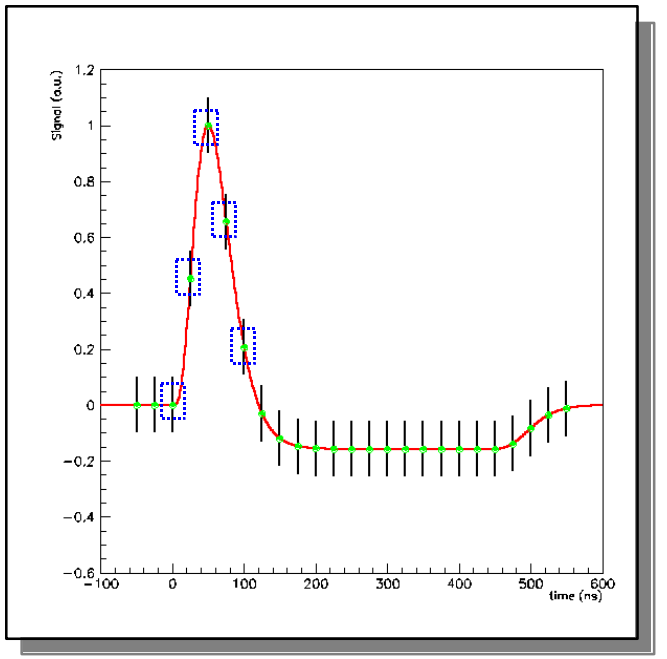
- receive and buffer the digitized samples from the FEB boards
  - typically 5 samples / channel
- perform online computations
  - energy for all samples
  - time, pulse shape quality for channels above a given energy threshold (*f* factor)
- format and make the data available for the LVL2 trigger
  - the raw data are replaced by calculated quantities at this stage
- and also:
  - data monitoring
  - collect and pre-process the calibration data

Multiple Sampling

$$E = \sum_{i=1}^{5} a_i \cdot (S_i - Ped)$$

$$E \cdot t = \sum_{i=1}^{5} b_i \cdot (S_i - Ped)$$

$$\chi^2 = \sum_{i=1}^{5} (S_i - Ped - E \cdot g_i)^2$$



... The ROD module

Design considerations

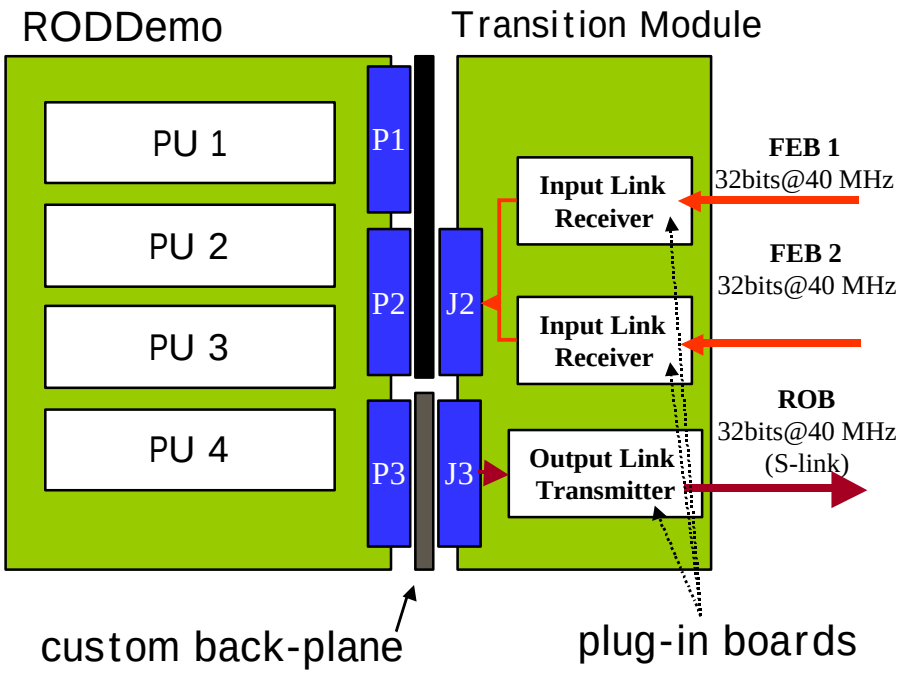
- The board should work at the LVL1 trigger rate of 100 KHz
  - average processing time per event is 10μs
- The processing time depends on the energy of the channel
  - it may have very large fluctuations, depending on the luminosity, the type of trigger and the calorimeter position (forward or barrel)
- The board should introduce minimal dead time in the readout at 100 KHz rate

- Our preference is to use commercially available programmable processors
  - A natural choice is **Digital Signal Processors (DSPs)**
    - efficient power in MAC type of calculations (filtering)
    - high I/O bandwidth
    - very fashionable; prices are dropping quite fast with continuously increasing performance

… The ROD module

The ROD Demonstrator

- VME64x 9U board
- input stream
  - two optical 1.28Gb/s links
    - 1.6Gb/s including protocol
  - 100 KHz event rate, ~320 Mbytes/s
- output stream
  - one copper/optical link (S-link)
  - average event size of ~1.6 Kbytes
- 4 DSP Processing Units (**PU**)
- VME interface for:
  - control: boot, configure,...
  - data readout: test beam, spy,...
  - monitoring: histograms,...

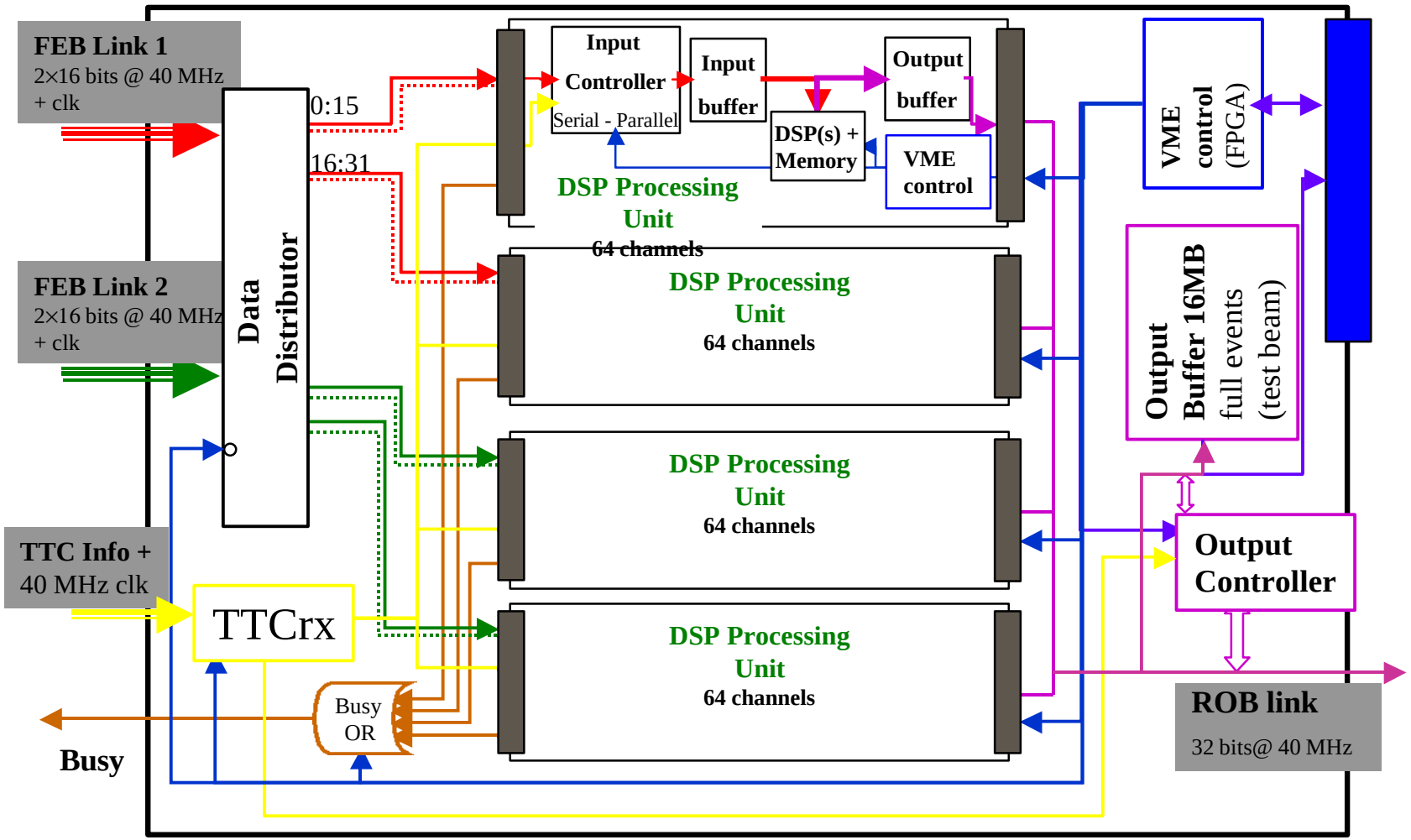


Collaborating institutes

LAPP Annecy, BNL, Columbia Univ, Geneva Univ., CPPM Marseille, KTH Stockholm, SUNY Stony Brook

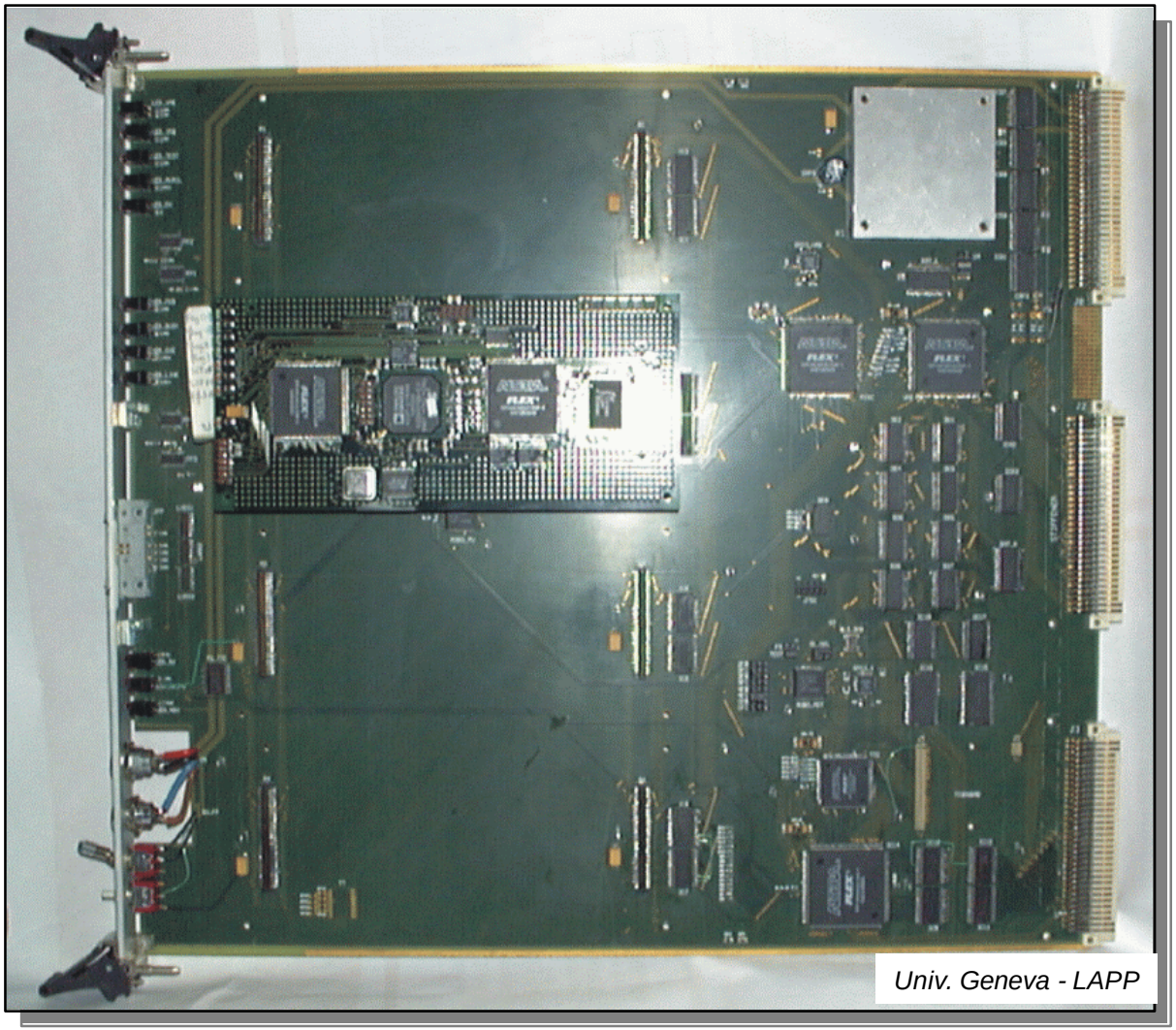
… The ROD module

The ROD Demonstrator board



… The ROD module

The ROD Demonstrator board



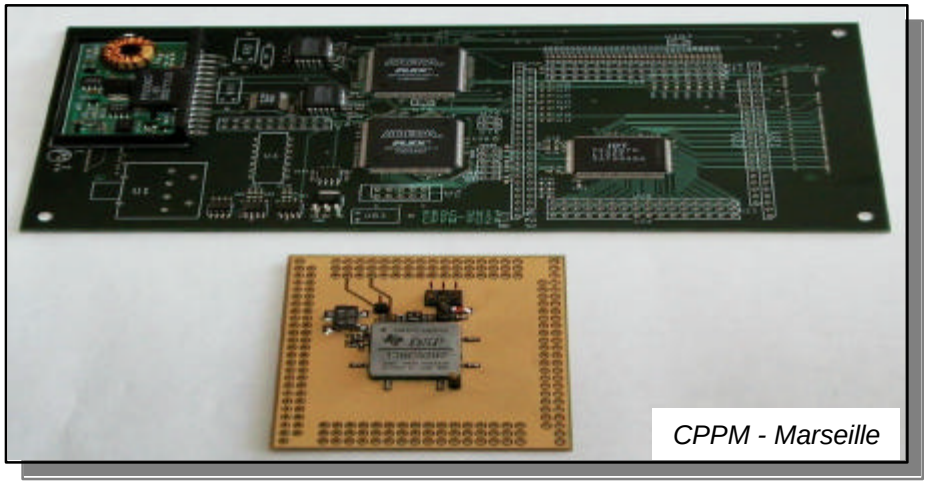
Univ. Geneva - LAPP

... The ROD module

PU Prototype

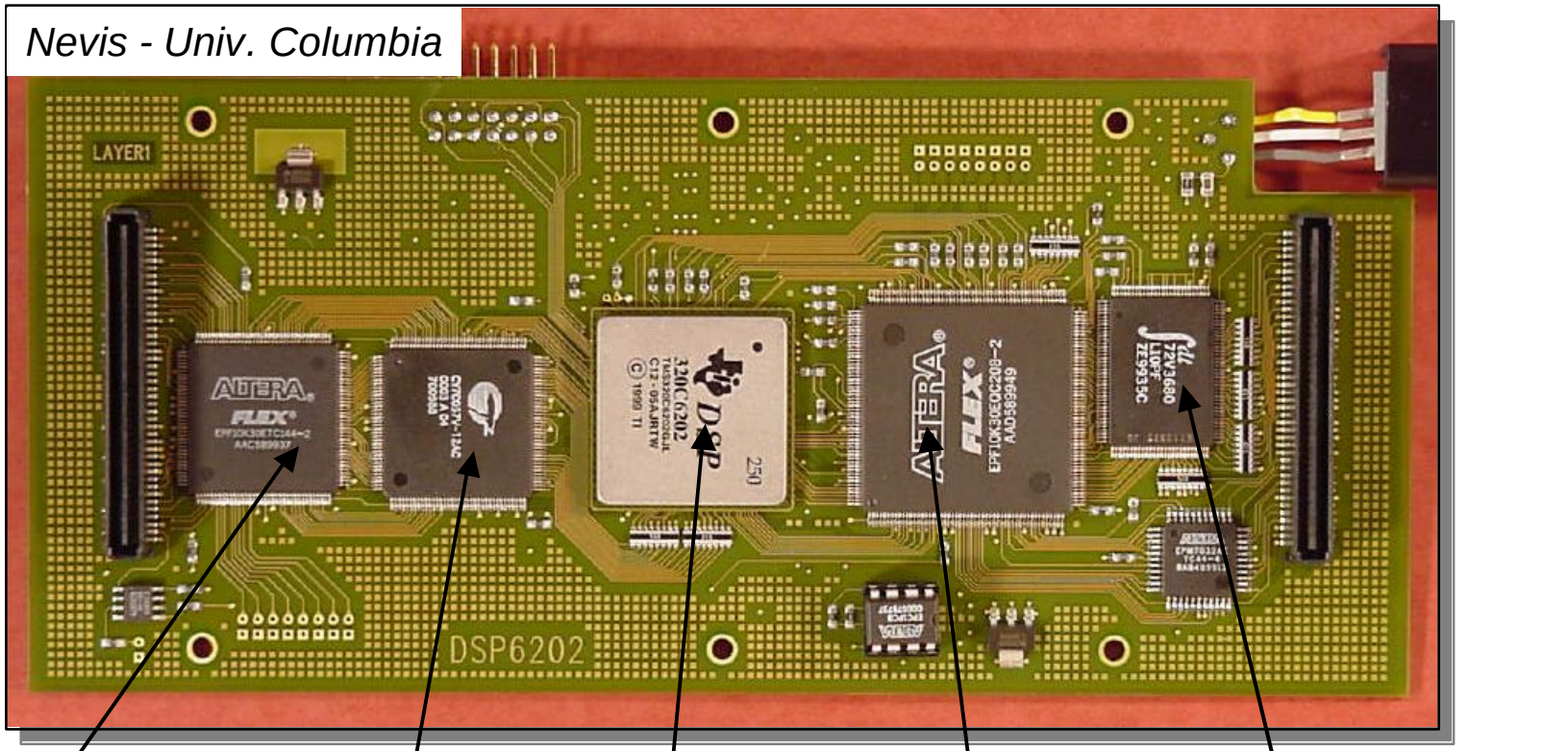
Texas Instruments 6202 DSP

- runs at 250MHz; 4ns core cycle
- integer arithmetic
- eight 32-bit instructions/cycle
- VelociTI™ Advanced Very Long Instruction Word (VLIW) 'C62x CPU Core
  - eight highly independent functional units:
    - six ALUs (32-/40-Bit)
    - two 16-Bit Multipliers (32-Bit Result)
  - load-store architecture with 32 32-bit general-purpose registers
  - instruction packing reduces code size
  - all instructions conditional
- 3Mbit internal memory
- 32-bit ext. memory interface (EMIF)
- 4 DMA channels
- 352-pin BGA package
- 3.3V I/O, 1.8V internal



… The ROD module

PU Prototype - Texas Instruments 6202 DSP

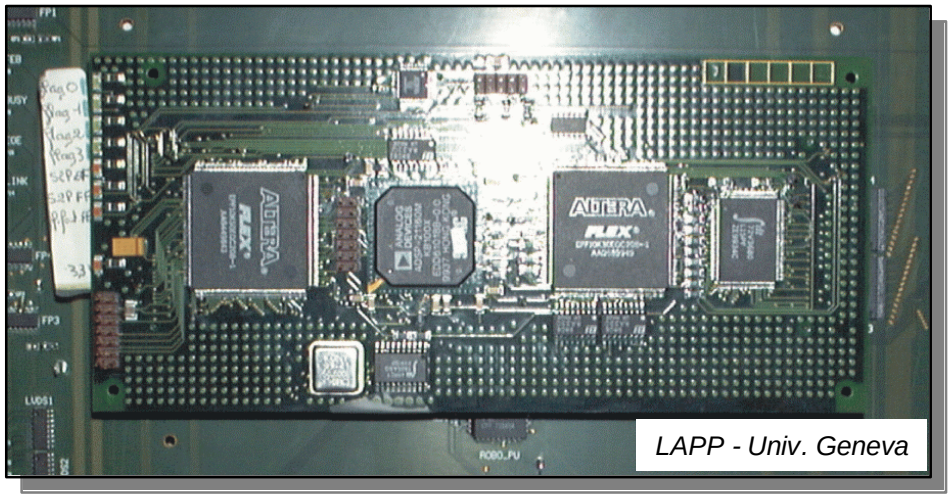


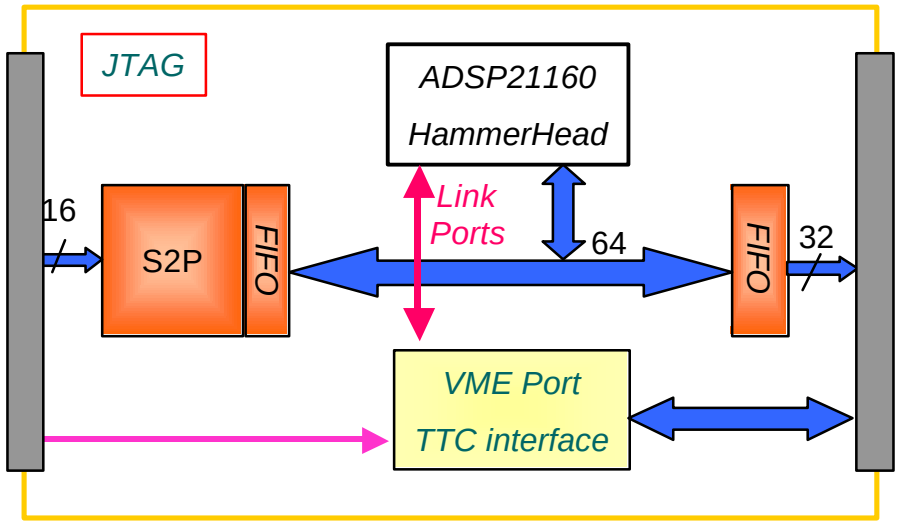
… The ROD module

PU Prototype

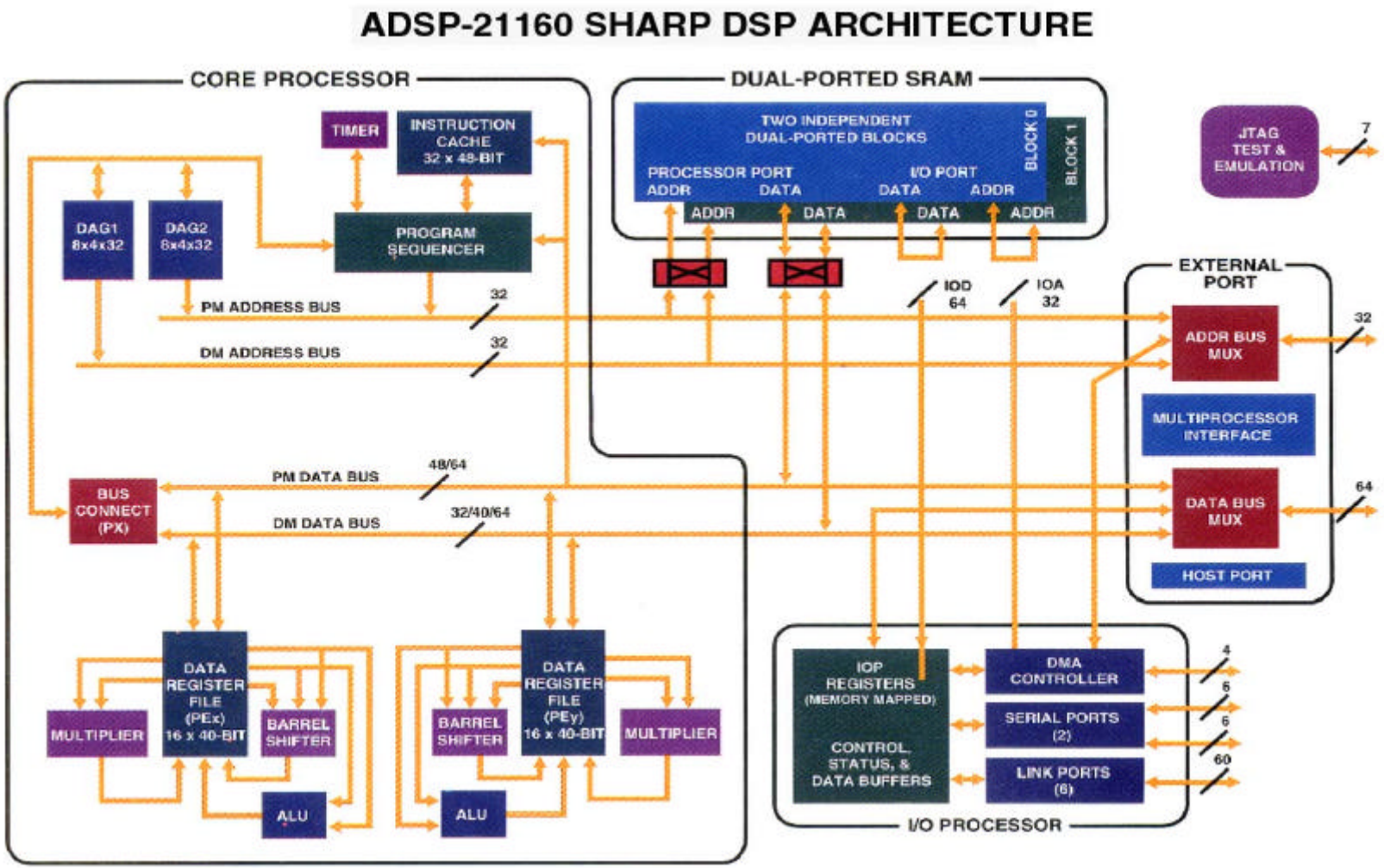
Analog Devices AD21160 DSP

- SHARC architecture
- 100 MHz, 10ns core cycle
- SIMD computational unit
- Floating point & integer arithmetic
- 4Mbits dual ported SRAM
- 14 DMA channels
- 6 (80MB/s) link ports
- 128 bits/cycle memory bandwidth





… The ROD module



... The ROD module

Status - Performance results

- all boards (MB + PUs) produced and tested so far in the lab
- the DSP based solution for the ROD is verified
  - comparable results for both DSPs

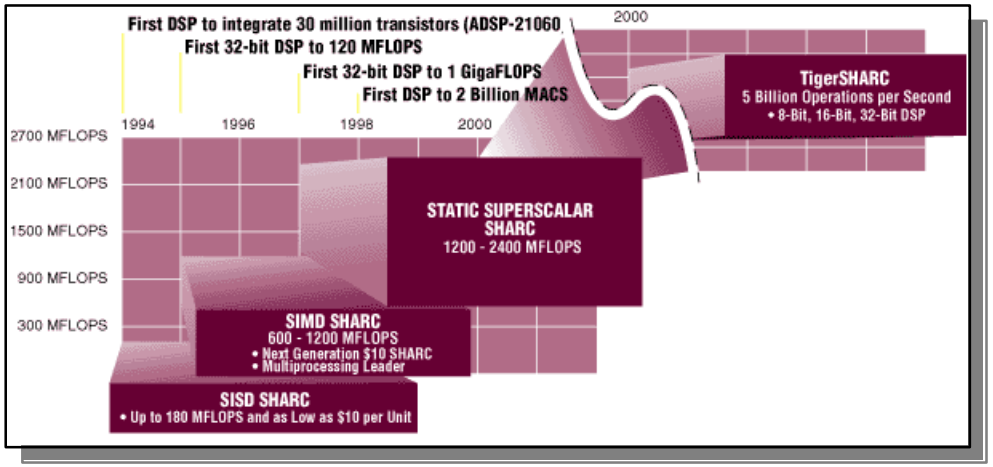
Processing time for 64 ch	*250MHz integer TI DSP*	*100MHz floating point AD DSP*
E, t, χ^2, **f=100%(10%)** Histogram, output format	~2750 cycles **11 (4.9) µs**	
E, t, χ^2, **f=10%** Histogram, output format		~990 cycle **9.9 µs**
Energy calculation precision	$2^{-16} = 10^{-5}$	$5\ 10^{-6}$

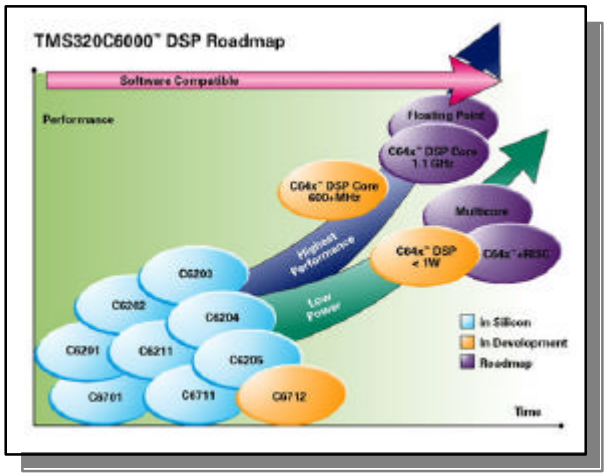
  - single S-link output stream bandwidth saturates at *f=10%*
- the TDR baseline architecture is feasible even with today's available DSPs
- further tests foreseen
  - test beam in '01 - HEC
  - ≥ 1 board test setups in progress (CERN/Geneva, BNL)

… The ROD module

The next steps

- evaluate new DSPs available in 2001





Analog Devices Tiger SHARC

- runs at 150MHz, 6.7ns instruction rate
- 1 to 4 instructions/cycle; max 6 instructions
- internal bandwidth of 7.2Gbytes/s
- SIMD operations with two computation blocks
- Dual computation blocks
- 6Mbit SRAM
- 64-bit generalized manipulation unit
- 6 single precision floating point or 24 16-bit fixed point operations/cycle
- 8 MAC/cycle peak 7.1MAC/cycle sustained 16-bit fixed point or 2 MAC/cycle peak and 1.8MAC/cycle sustained 32-bit

Texas Instruments C6203

- same as the C6202 but at higher clock frequency (300MHz, 3.33ns instruction rate) and with additional internal memory (7Mbit SRAM)

> *"… In fact a quick analysis of the myriad of new product introductions over the past year or so will show that DSP has become the technology driver for the entire semiconductor industry."* **W.Strauss, Forward Concepts Tempe AZ**, RTC Magazine, March 2000

… The LArgon read-out driver (ROD) module

… The next steps

- Given the present results and the expected performance figures of the new DSPs:
  - evaluate the possibility to double the channel density per PU
    - single PU (single DSP) to treat 128 channels (a complete FEB)
  - and also double the number of PUs in the board
    - eight PUs per ROD module
- A careful study should be made, but first indications show it is not impossible
  - in industry we find today boards with up to 8 DSPs (but I/O?)
  - obvious advantages:
    - more compact system, shorten production, testing and installation times, easier to maintain, potential cost savings
- Interesting R&D project until end '01 when final architecture design needs to be frozen
- Final ATLAS ROD should be ready by end '02

Summary

…on the readout architecture of the ATLAS LArgon calorimeters

FEB

- Design nearly frozen
- Final design boards successfully tested in the test beam
- Radiation hard (DMILL) versions of the components being made at present

Front-end links

- several options studied
- heavy test beam and radiation hardness tests
- single G-link solution adopted

ROD

- Fulfillment of ROD Demonstration Project to test prototype evaluation modules for the current leading DSPs
- Performance results indicate that the design architecture (TDR) is feasible even today.
- Coming year: Aggressive R&D program with the new more powerful DSPs available in short term to before freeze the final design.