Triggering and Calorimetry

Calor2000

October 9-14, 2000

Annecy, France

Outline

- Triggering in Collider Experiments
  - CDF and D0
  - ATLAS and CMS
- Calorimetric Triggering at Level 1
- FPGA's in Triggering
  - Advantages
  - Examples of Implementations
- Summary

Common Detector characteristics

- Projective towers in η and ϕ
- Separate Electromagnetic and Hadronic Calorimetry
- Nearly Hermetic Coverage

Common Trigger Features

- Multiple Level Triggers
  - Level1 - Hardware, pipelined; latency ~μsec
  - Level 3 - General purpose processors
  - Level 2 - Virtual or specialized processors
- Trigger Inputs at Level 1
  - Calorimeter information at reduced granularity
  - Muon information

Lvl1 Input Comparisons

	Cal EM/H	Muon	Tracking	Correlation
CDF	X	X	X	Cal/track **15° Wedges**
D0	X	X	X	Cal/track $2\pi/4$
ATLAS	X	X		
CMS	X	X		

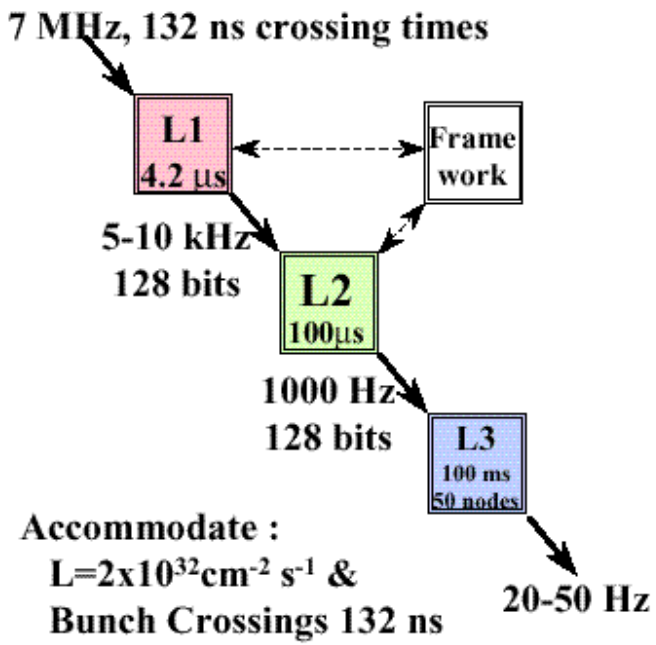
L1 Granularity ($\Delta\eta x\Delta\phi$)

	EM	JET	TAU
D0	0.2x0.2	0.2x0.2	x
CDF	0.2x0.2	0.2x0.2	x
ATLAS	0.1x0.1	0.4x0.4,0.6x 0.6,0.8x0.8	0.4x0.4
CMS	0.087x0.087	1.04x1.04	0.35x0.35

Architecture Comparisons

	Level 1	Level 2	Level 3
CDF	Pipelined; 4 μs latency	Special Processor; 100 μs latency	Farm
D0	Pipelined; 4.2 μs latency	Special Processor; 100 μs latency	Farm
ATLAS	Pipelined; 2 μs latency	ROI based, spec. proc. ~ ms latency	Farm
CMS	Pipelined; 3.2 μs latency	Virtual; ~ ms latency	Farm

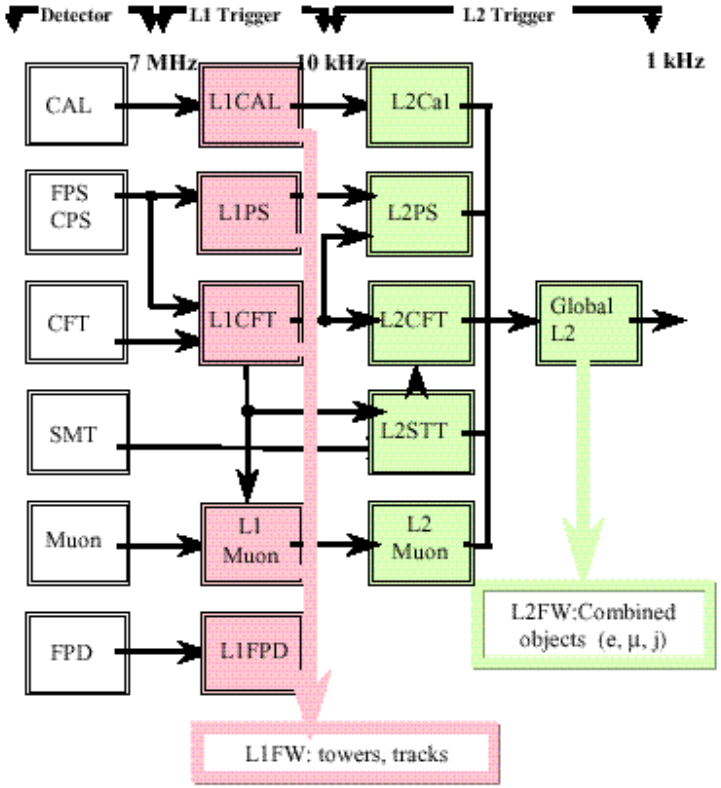
The DØ Trigger



Accommodate :
$L=2x10^{32}cm^{-2}s^{-1}$ &
Bunch Crossings 132 ns

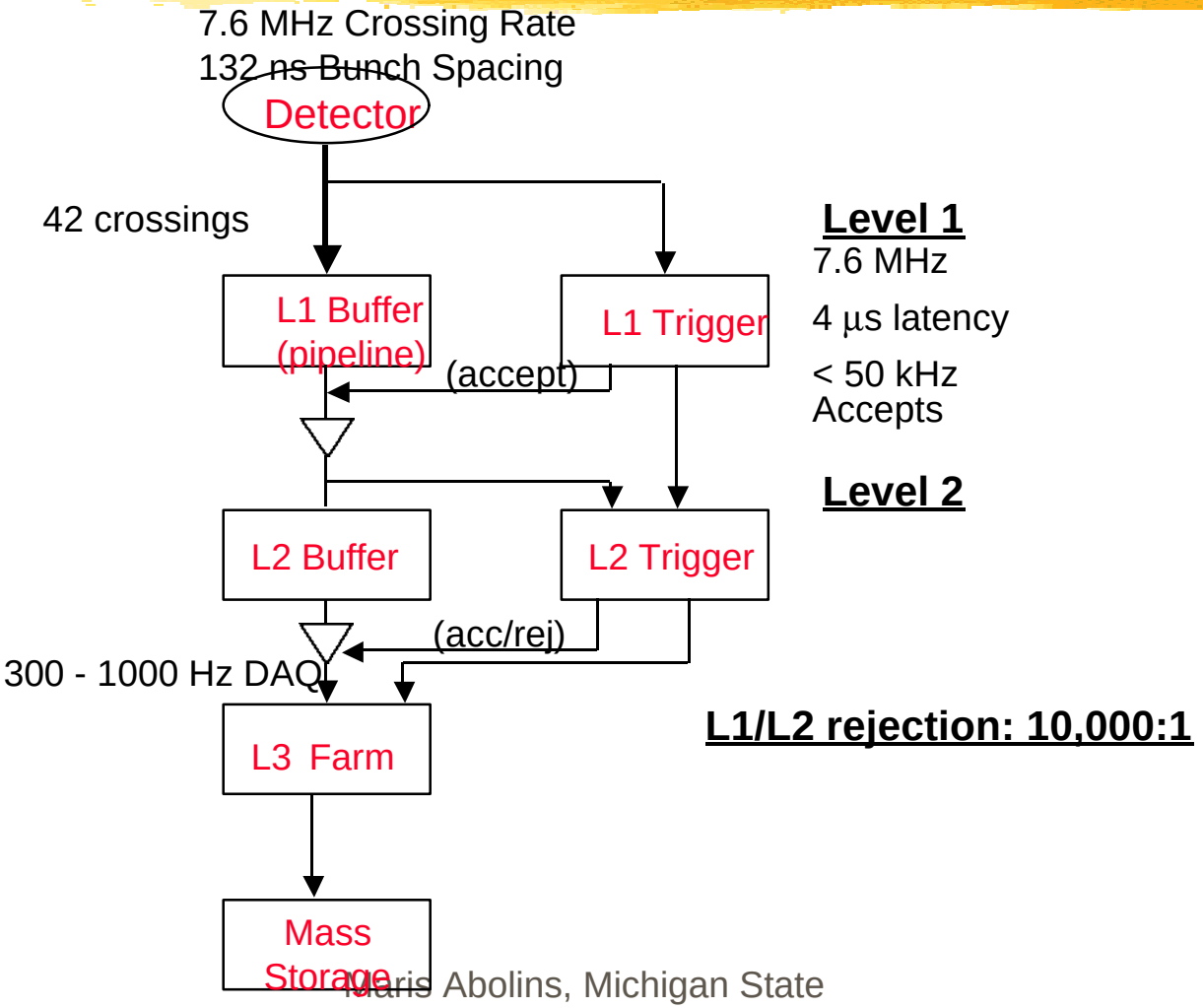
Maintain Run I e, jet, m acceptance

Deadtime: <5%

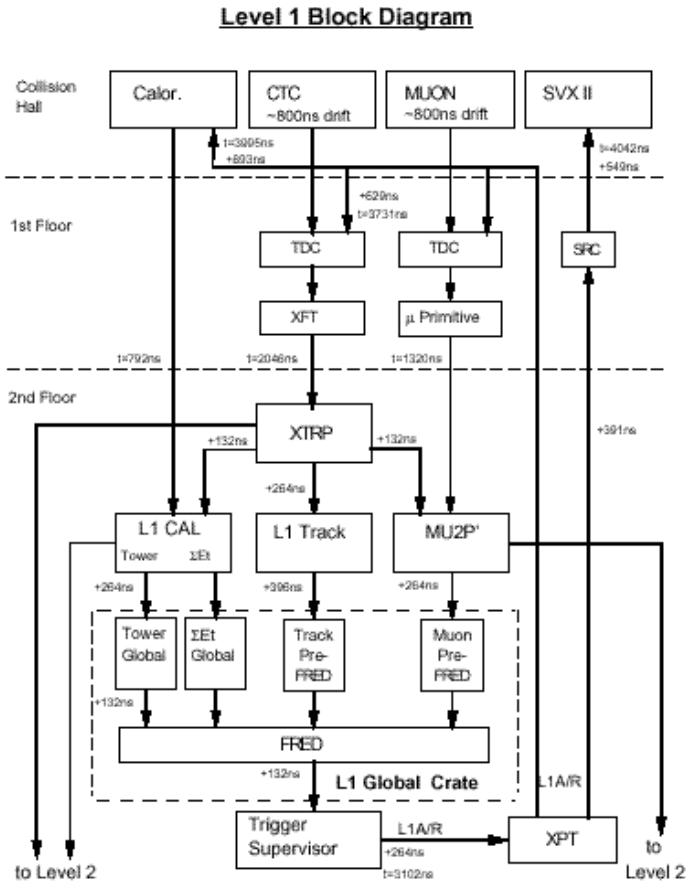


L1 Trigger Status/Issues

CDF Trigger


7.6 MHz Crossing Rate
132 ns Bunch Spacing
Detector
42 crossings
L1 Buffer (pipeline)
L1 Trigger
(accept)
Level 1
7.6 MHz
4 μs latency
< 50 kHz Accepts
Level 2
L2 Buffer
L2 Trigger
(acc/rej)
300 - 1000 Hz DAQ
L3 Farm
L1/L2 rejection: 10,000:1
Mass Storage

CDF Level 1 Block Diagram



CDF/DØ Trigger Differences

CDF

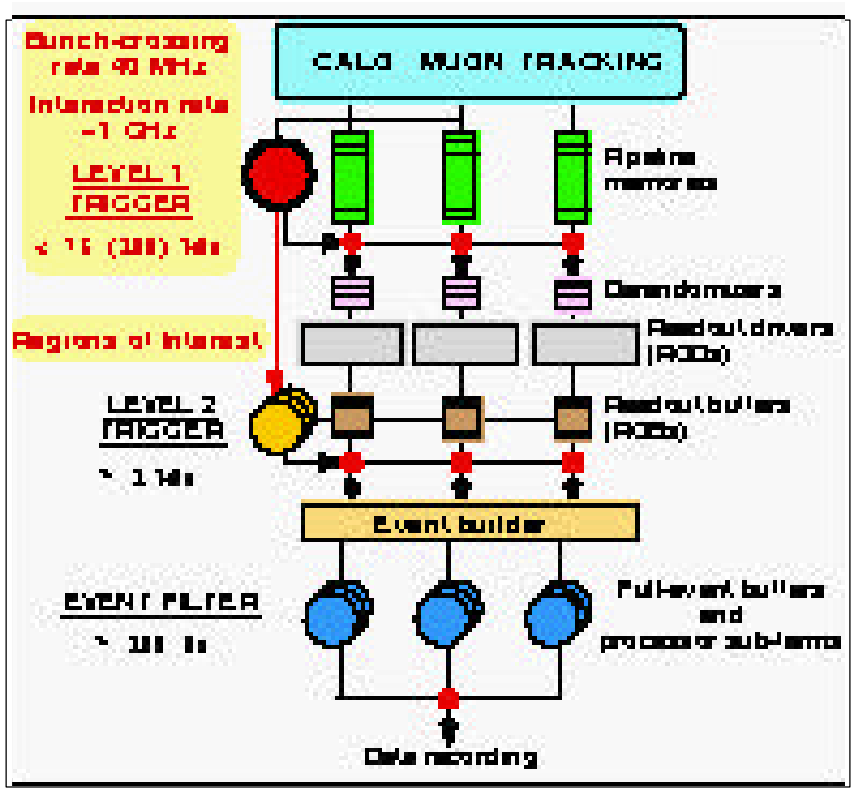
- L1 Accepts <50 kHz
- Track/Cal correlation at L1 to $\pi/12$ degrees
- Silicon displaced vertex trigger at L2

DØ

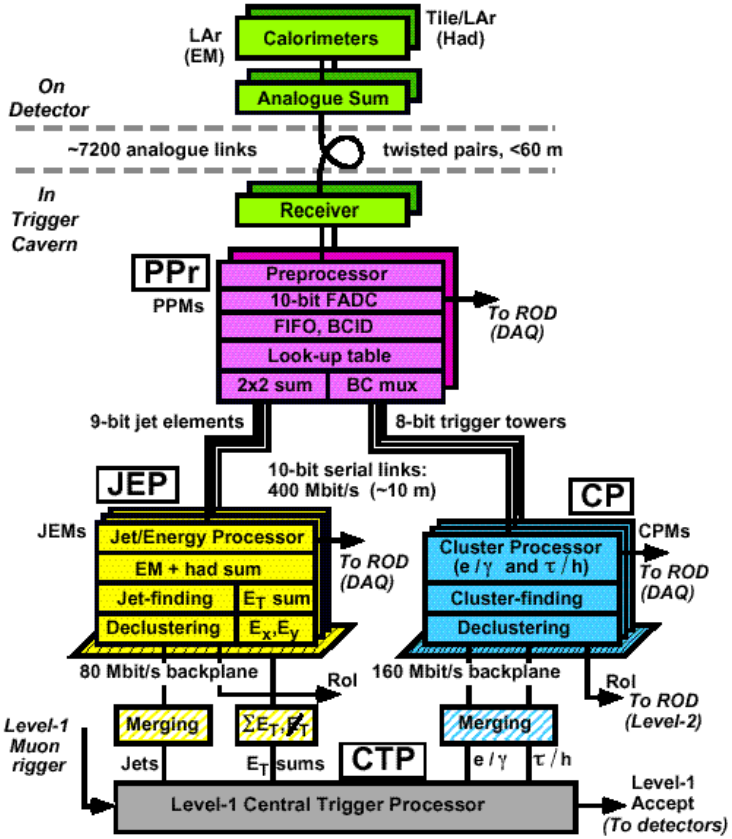
- L1 Accepts <10 kHz
- Track/Cal Correlation at L1 to $\pi/2$
- Silicon displaced vertex trigger at L2 - but delayed

ATLAS Trigger Overview

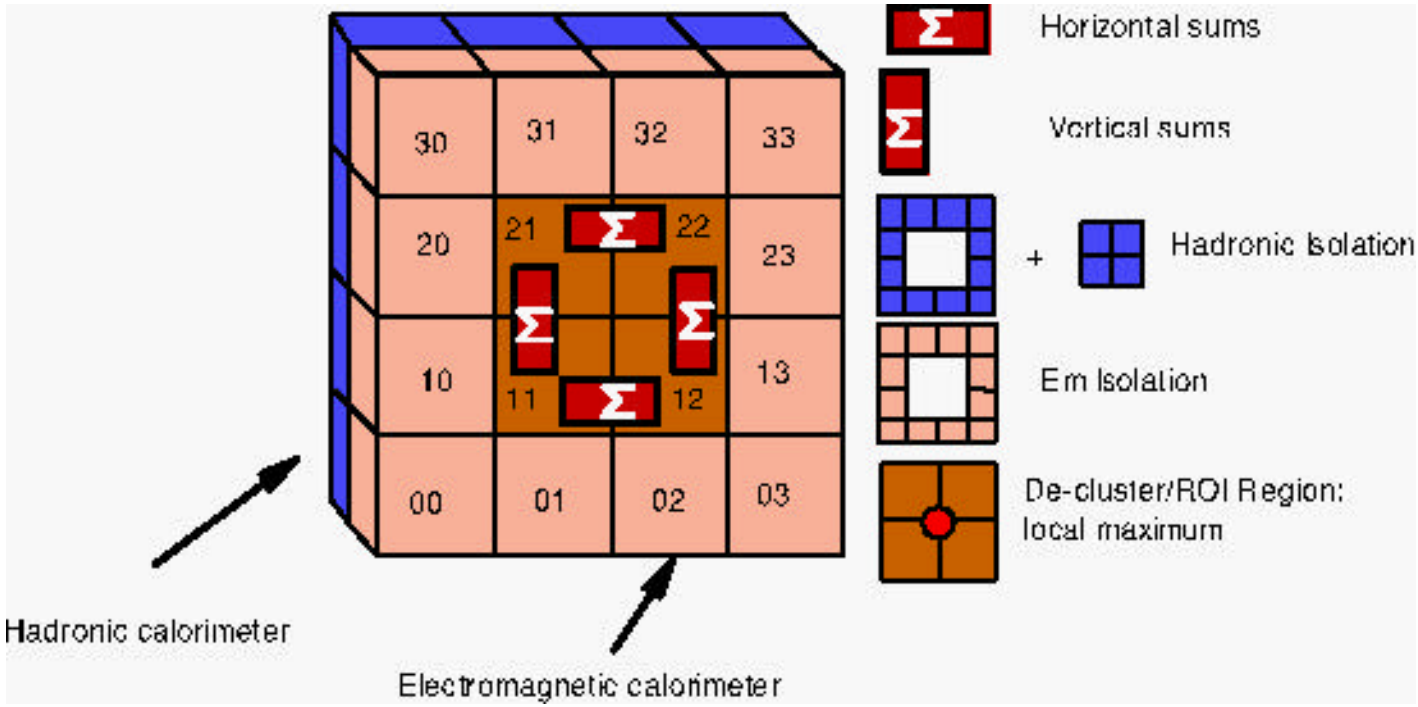
- Mult-level trigger
  - 40 MHz->100 kHz->1 KHz->100Hz
- Lvl1
  - Latency - 2 μs
  - Calorimeter & Muon
  - Central Trigger Processor
- Lvl2
  - Full granularity
  - Regions of Interest
- Event Filter - Full reconstruction



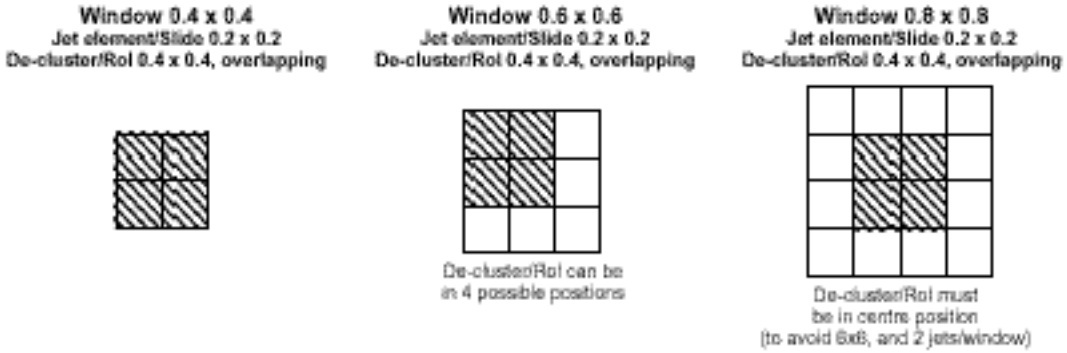
ATLAS Level 1 Calorimeter Trigger



ATLAS LVL1 EM Trigger

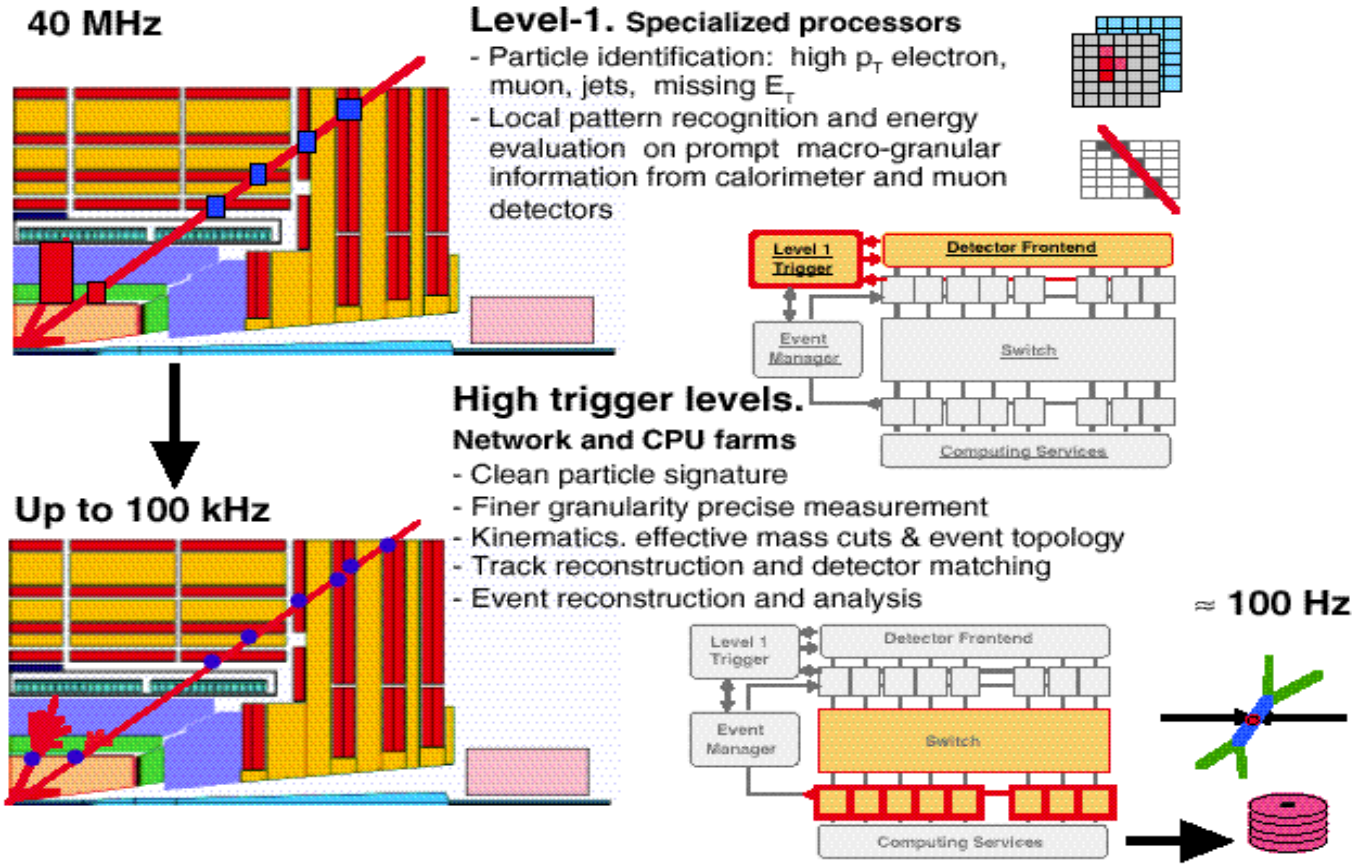


LVL1 Jet Trigger

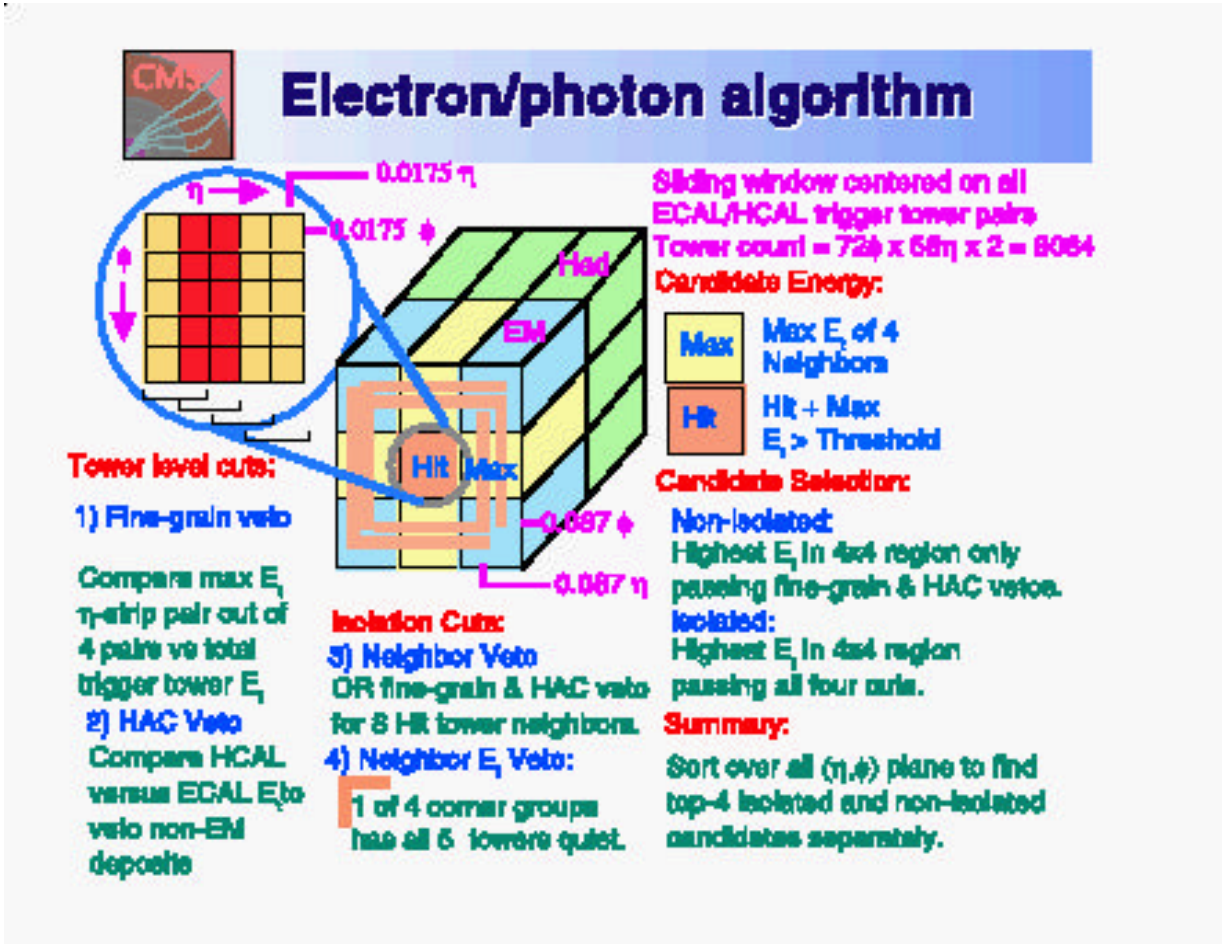


Maris Abolins, Michigan State University

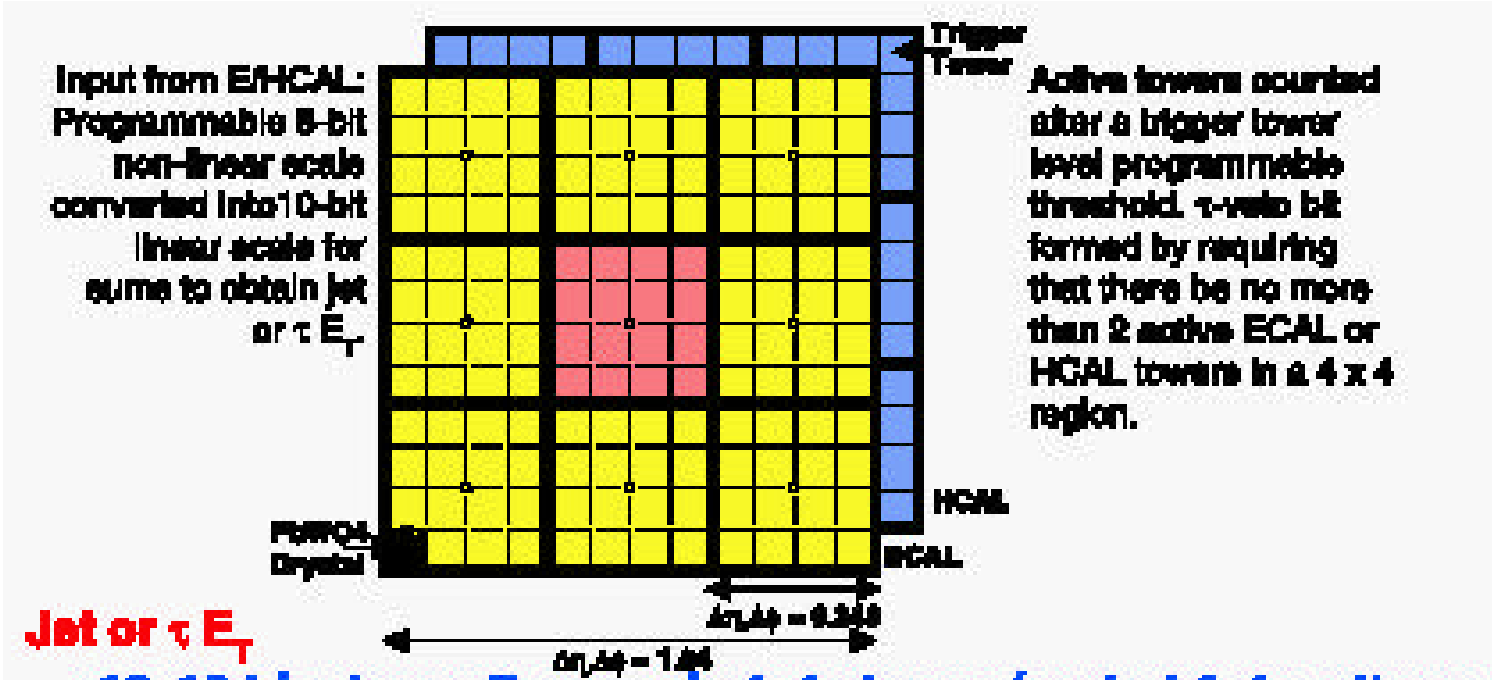
CMS Trigger


40 MHz
Level-1. Specialized processors
- Particle identification: high p_T electron, muon, jets, missing E_T
- Local pattern recognition and energy evaluation on prompt macro-granular information from calorimeter and muon detectors
Level 1 Trigger
Detector Frontend
Event Manager
Switch
Computing Services
High trigger levels.
Network and CPU farms
- Clean particle signature
- Finer granularity precise measurement
- Kinematics. effective mass cuts & event topology
- Track reconstruction and detector matching
- Event reconstruction and analysis
Up to 100 kHz
≈ 100 Hz
Level 1 Trigger
Detector Frontend
Event Manager
Switch
Computing Services

CMS EM Trigger



CMS Jet Trigger



Jet or τ E_T

- 12x12 trig. tower E_T sums in 4x4 steps w/central 4x4 > others

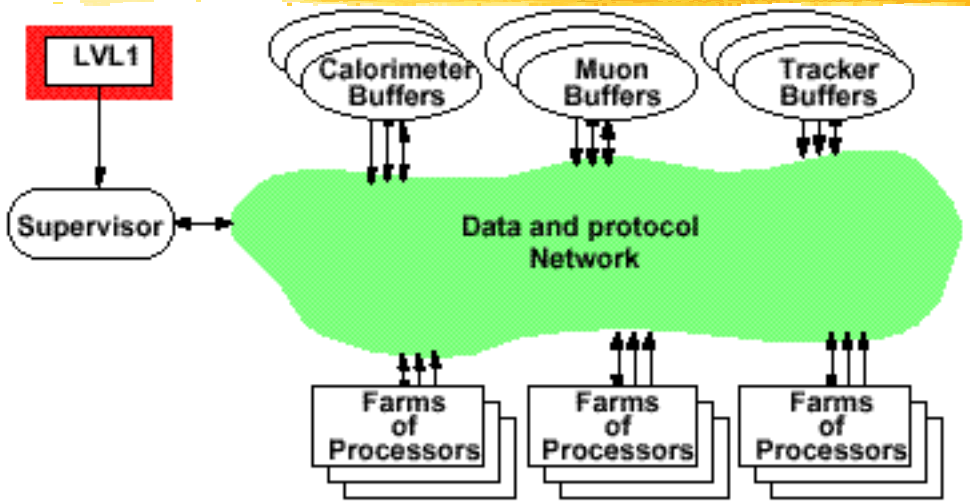
τ algorithm (isolated narrow energy deposits)

- Redefine Jet as τ if none of the 9 4x4 region τ-veto bits are on

Output

- Sorted top 4 jets & top 4 τ-jets & counts of jets

ATLAS/CMS Trigger Comparisons



- Level 2 Trigger
  - ATLAS - Region of Interest processing ~few % of data
  - CMS - Virtual Level 2 - transfer data as needed
- Switch
  - ATLAS - Possibly separate physical switches for Lvl2 & DAQ/EF
  - CMS - One large switch
- Tradeoffs - Complexity vs. switch and link bandwidth

FPGA Advantages

- Rapid Development
  - Relative to ASICs - days or weeks not months
  - Errors easy to correct
- Flexibility
  - New ideas or changes easy to implement
- Speed and Size
  - > Moore's Law Growth in # gates
  - Fast clock speeds possible
- ASIC vendors increasingly reluctant to accept complex, low volume jobs

FPGA's in Triggering

- CDF - Extensive use of FPGA's e.g. in Trigger Decision Logic
- D0 - Trigger Framework, including Decision Logic and Scalers based on FPGA's
- ATLAS
  - Level1 trigger uses mainly FPGA's in place of ASIC's.
  - Atlantis project
  - Region of Interest Builder Card Designed with FPGA's

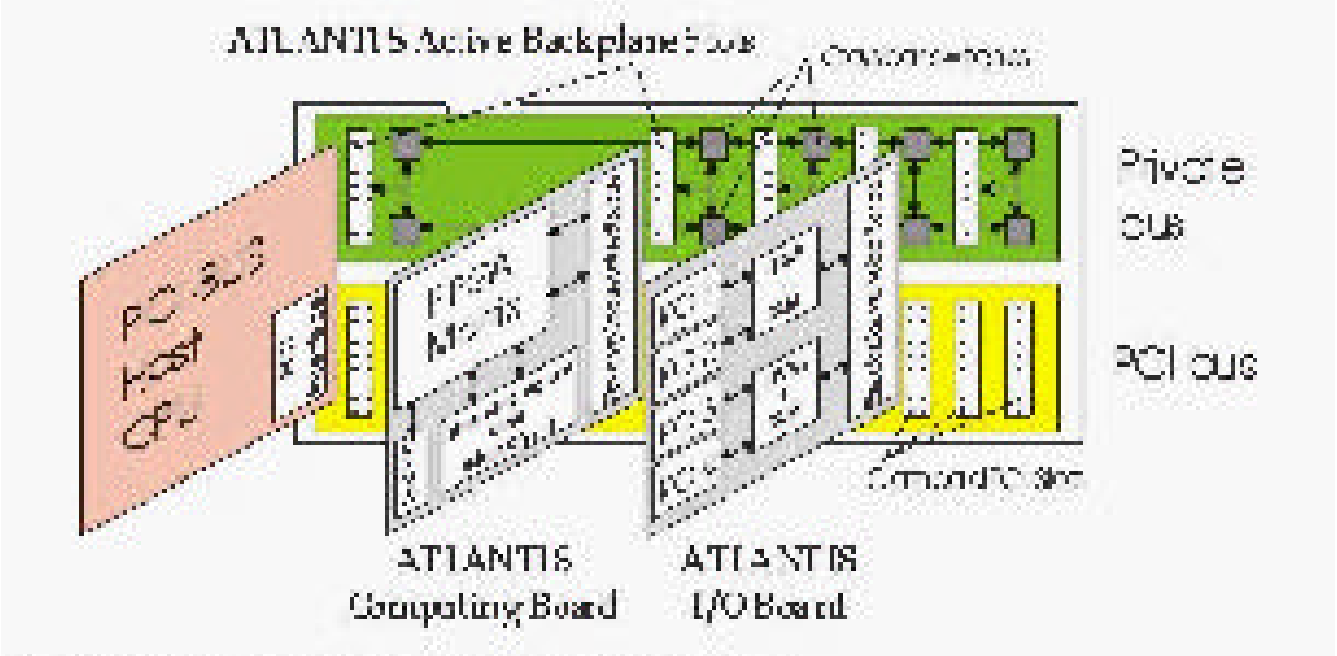
Recent Progress in FPGA's

- Gate Counts - from 10^4 to $>10^6$ in < 5yrs
- Speed - as fast as 600 MHz
- Pin Counts > 1000. DLL - Bit serial input
- Power Reduction - 1.5 V parts available
- Large quantitites of On-board RAM
- Embedded functions - PCI interface, RISC microcontroller, Power PC cores, etc.

FPGA use in DØ: Quad Matching

- Match tracks or preshower with calorimetry ($\pm\eta$, $2\pi/4$)
- Desirable for low ET electrons e.g. from J/Ψ decays
- Gives x 2 - 3 rate reduction for low E_T jets/electrons
- Need not foreseen in original design
- Decision logic in FPGAs: 256 input terms->128 triggers
- Need to construct new terms e.g. $\Sigma_\alpha(C_\alpha \times T_\alpha)$ wher C is calorimeter term and T tracking
- Use original decision logic card with larger FPGA from XC4000 family of devices
- Crucial factors: Increased size & reprogrammability

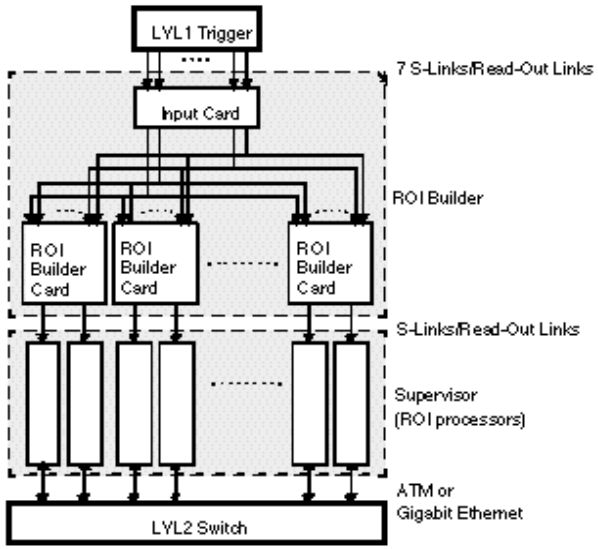
ATLAS - Atlantis(Uni. Mannheim)

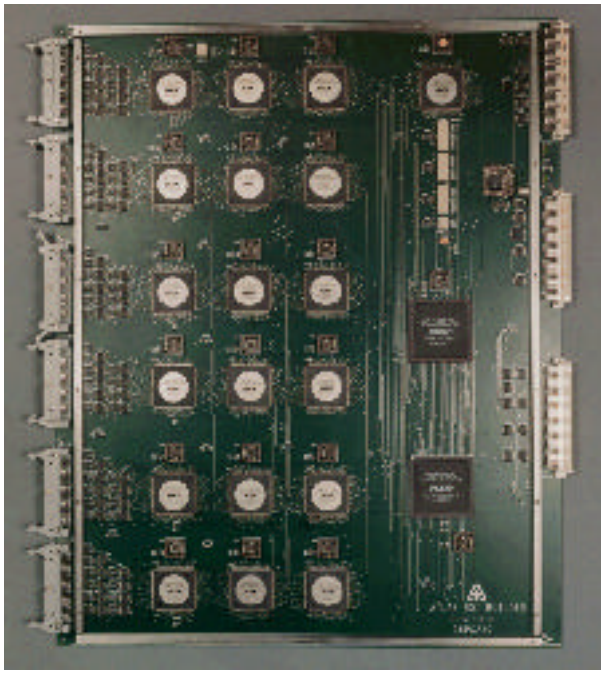


Atlantis

- Modular, Hybrid FPGA/CPU processor
- 1.4 GB/s I/O capacity per board
- Powerful FPGAs: Orca 3T125, Virtex XCV600
- CPU: CompactPCI-based standard PCU
- RAM sub-boards
- Interconnect: CompactPCI + private bus
- Proposed ATLAS application: LVL 2 B-Physics Triggers
  - TRT Track Finding
  - Performance Improvement x 20 over standard PC

ATLAS Lvl1 RoI Buider (ANL, MSU)





RoI Builder

- Modular, parallel design using Altera10K family of FPGAs
- Each card receives as many as 12 input streams of RoI fragments, assembles them into output records for transfer to two Supervisor processors
- Design is manifestly scalable
- Demonstrated to operate at 100kHz - the maximum Level 1 Trigger Accept Rate at ATLAS

DØ L 1 Cal Trigger Uprade

- Run at 132 ns crossing rate (8 MHz)
- Basic Granularity 0.2x0.2 ($\Delta\eta x \Delta\phi$)
- EM Max in 2x1 towers with isolation and H veto
- Hadron Max in 5x5 tower area
- Displace Mask by 1 tower in η or ϕ
- Cover all calorimeter: 40x32 towers

Exercise: Duplicate Run I L2 in L1

Run I

- DSP's: 11 C40's
- Data: 512 bytes
- Clock: 40 MHz
- No Pipelining
- Latency: ~100 μs
- Code: High Level language e.g. C with optimizations

Run IIB

- FPGA's: 11 e.g. Virtex-E
- Data In
  - 512 bytes on 512 pins
  - Bit serial at 8x8 = 64 MHz
- Pipelining in FPGA
- Latency ~few μs
- VHDL programmable

Conclusions

- Powerful and fast electronic devices available for future triggering
- Intelligent, reconfigurable triggers are an attractive possibility
- Extremely compact triggers will be limited only by cabling of inputs and by power density on card