The *KLOE* calorimeter front end electronics

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for the KLOE collaboration

Presented by
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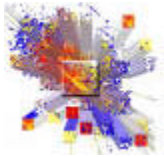
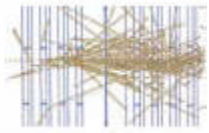
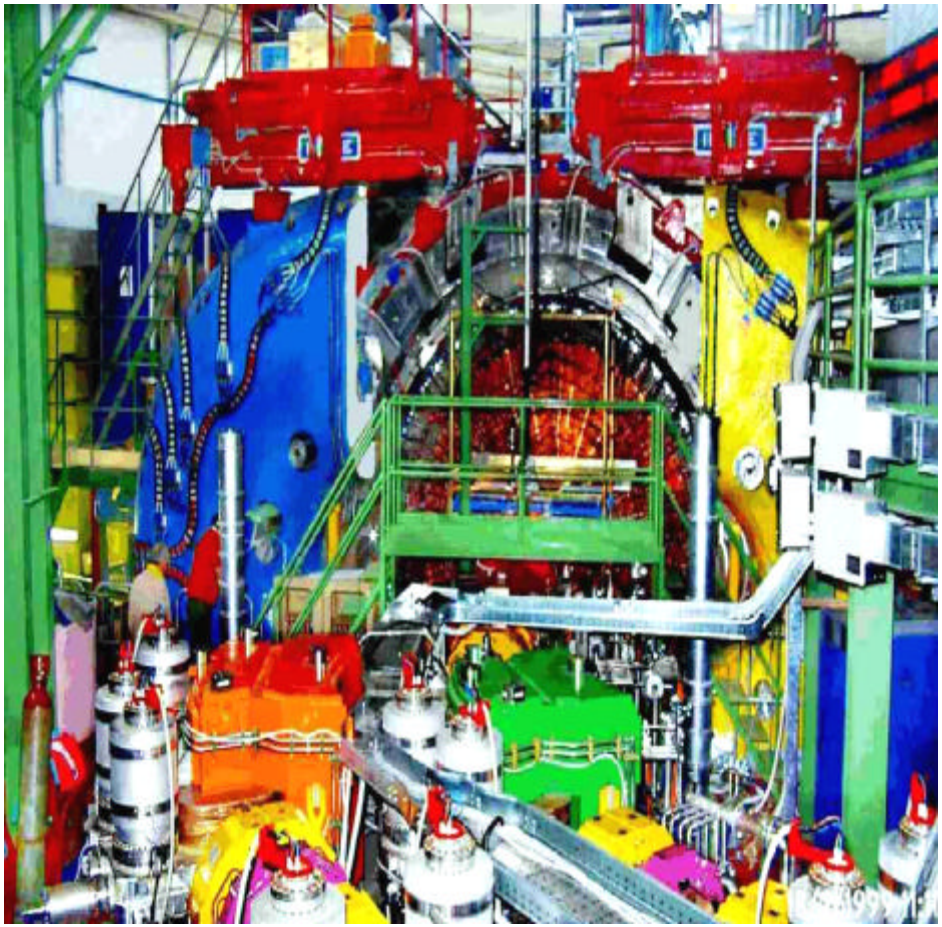


IX International Conference
on Calorimetry in Particle Physics
CALOR2000



Outline

- *Requirements*
- *EMC FEE chain*
  - *Preamplifier*
  - *SDS board*
  - *Adc*
  - *Tdc*
- *Performances*
- *Conclusions*



The KLOE experiment in the DAΦNE hall

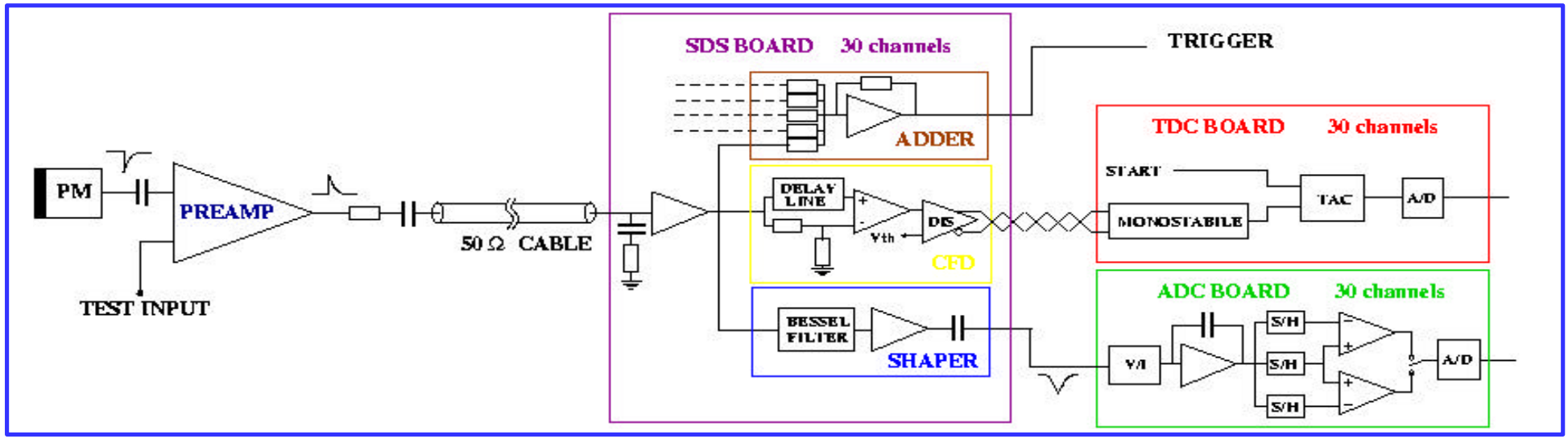
Requirements

The **KLOE** goal is to measure $\hat{A}(e\ell/e)$ to $\sim 10^{-4}$

- Energy resolution
  $\sigma(E)/E \sim 5\%/\sqrt{E(\mathrm{GeV})}$
- Full efficiency
  $20 < E_\gamma < 300$ MeV
- Time resolution
  $\sigma(t) \approx 70\ \mathrm{ps}/\sqrt{E(\mathrm{GeV})}$
- Spatial resolution
  ~ 1 cm for γ conversion point

- High resolution in time and energy
- Low noise (< 1 p.e.)
- Low time jitter (< 25 ps)
- Good bandwidth and dynamic range
- High long term stability and linearity (< 0.5%)
- Low dead time (< 2.3 μs)

The FEE chain



- 4880 PM signals
- 492 FEE boards (SDS+ADC+TDC) with a modularity of 30 channels
- 12 9U crates for SDS with custom crate controller
- 40 custom linear power supply modules for SDS and preamplifier
- 24 9U-VME crates (ADC -TDC) with crate custom bus (AUX-bus)
- 4 chains with two inter-crate connecting buses
  - Slow speed commercial bus (VIC-bus) to initialization and test purposes
  - Fast speed custom bus (C-bus) for data read-out (50 Mbytes/s)

Preamplifier

Why the preamplifier

- Drive a 50 Ω coax-cable
  - Back and forward termination
  - Transmission of fast pulses with minimal ghosts
- Reduce the PM anode current
  - Guarantee PM pulse linearity
  - Preserve PM gain stability

Specification

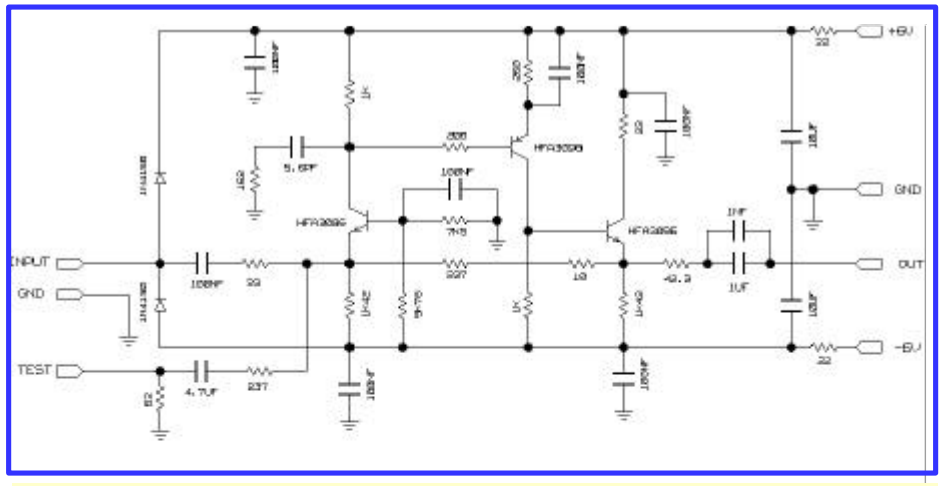
- Low noise
- Good dynamic range
- High reliability
- Low power
- Low cost

Discrete solution with only three transistors

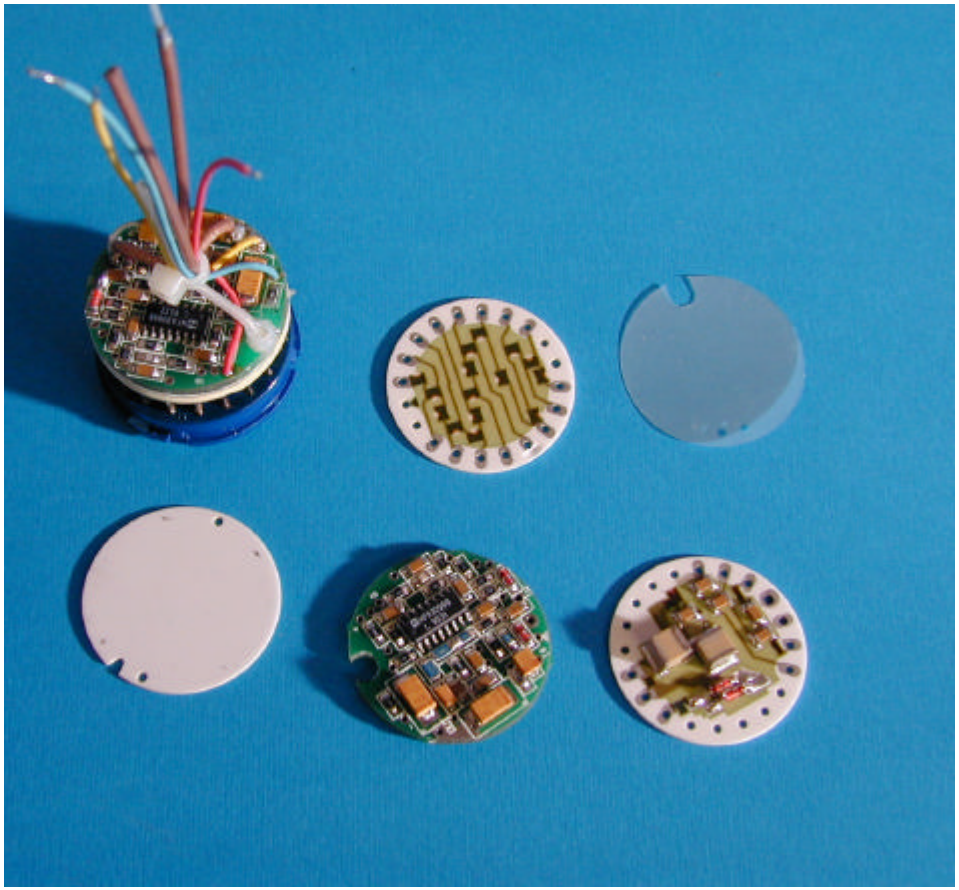
Three stages in current feedback configuration

Good layout and smd technology

Preamp performances

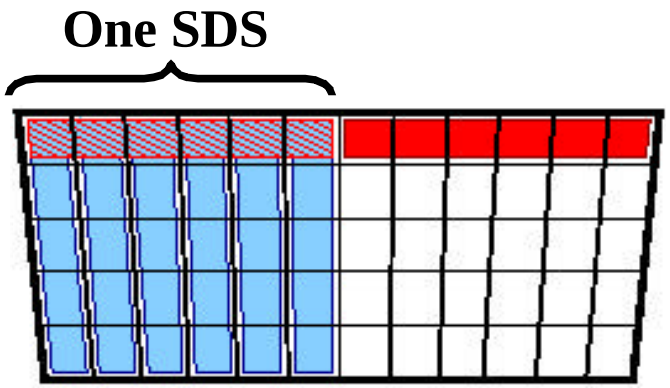


- Conversion gain 247 V/A
- PM signal rise time ~ 2 ns
- Max input signal ~ 20 mA
- Max output signal 5V
- Non-linearity < 0.2%
- Power dissipation < 60 mW
- Test input



SDS board

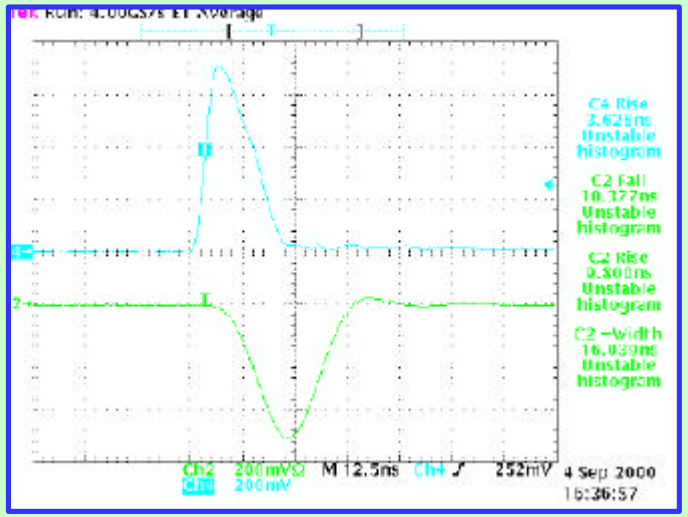
- Shape signal for ADC
  - Passive third order Bessel filter
    - Compensate cable distortion
    - Stretch the pulse
      - Reduce ADC bandwidth
  - Amplifier to tune chain gain
- Discriminate signal for TDC
  - Constant fraction discriminator
    - Minimize time walk
  - Differential current output signal
    - Reduce stray elements and cable resistance effects on the rise edge
    - Increase common mode noise rejection
- First trigger stage
  - Reduce calorimeter granularity
    - Sum 5 PM signals of the same tower of the calorimeter module
  - Implement cosmic veto
    - Sum PM signals of outer plane of calorimeter module

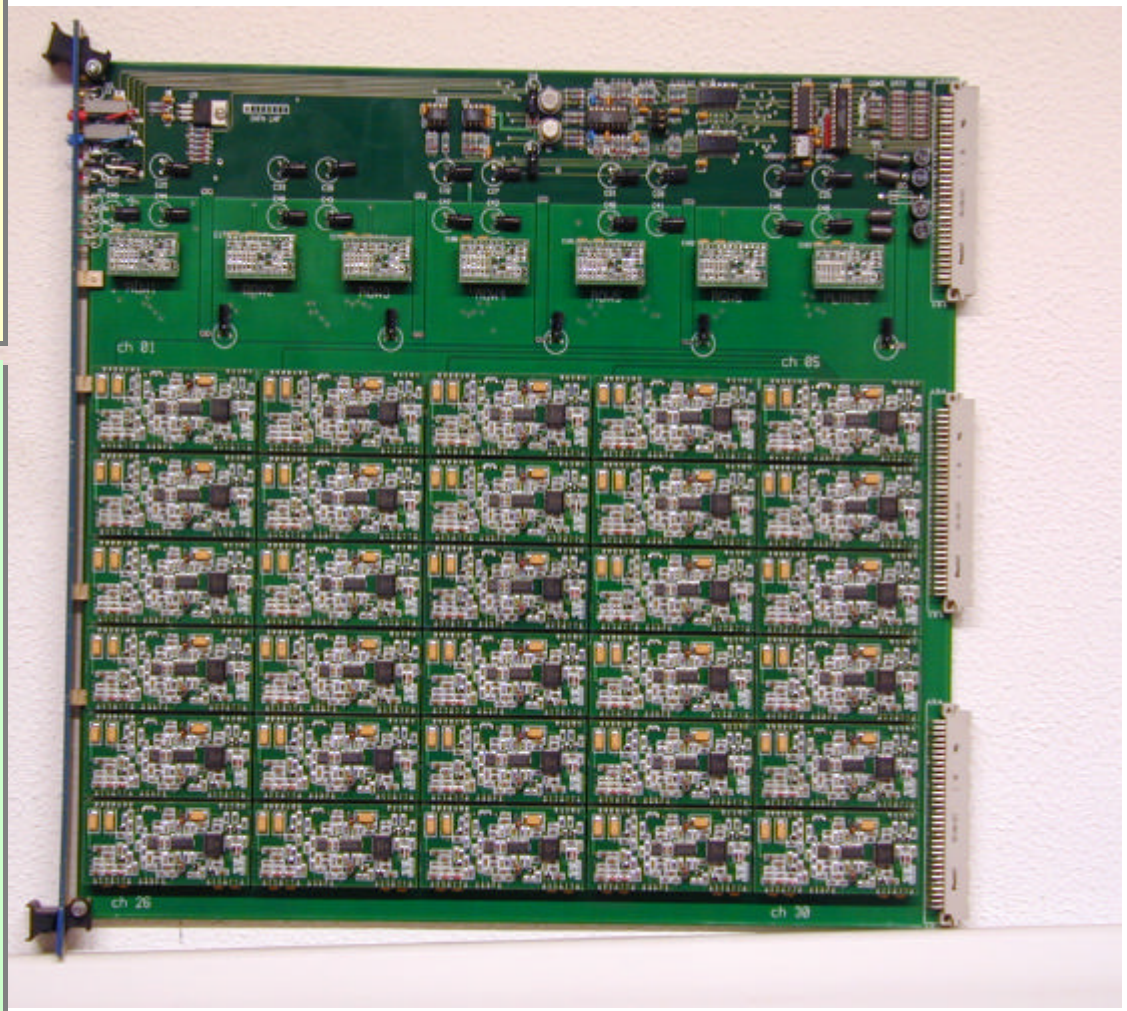


SDS performances

- Time walk < 200 ps
- Threshold ~ 4÷5 mV (3÷4 MeV)
- Output rise time 1.2 ns
- Neighbouring channels cross-talk
  ~ -40 dB

- Output fall time ~10 ns
- Output signal FWHM ~16 ns





Signal arrival time

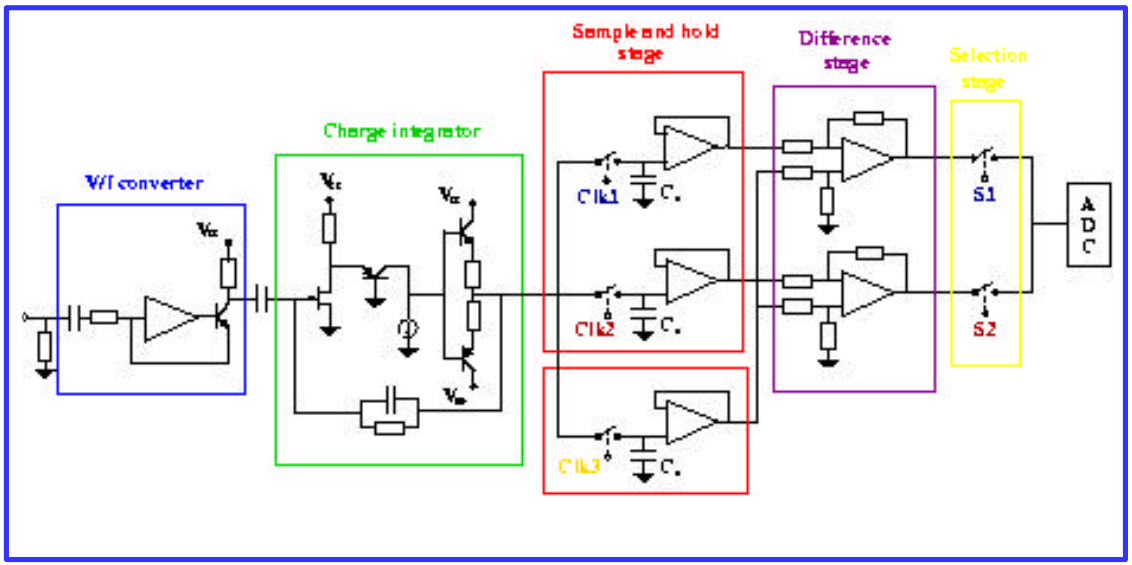
- Signals arrive at the input of ADC and TDC before the trigger at no fixed time
  - can precede the trigger by as much as 350 (220) ns
    - KLOE physic
    - Trigger generation
    - Cables
  - Arrival time windows for all particles of an event must be ~ 200 ns

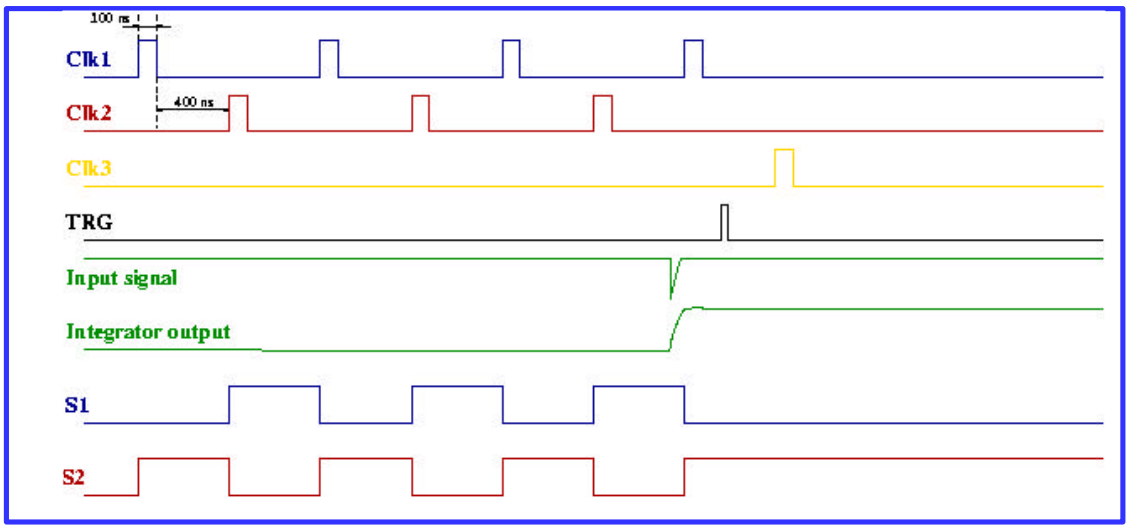
NO integrated delay line ⇒ MISSING MAGNETIC FIELD

NO long coax-cable ⇒ ROOM and COST

ADC Double baseline sampling and difference technique
TDC Delay with monostable

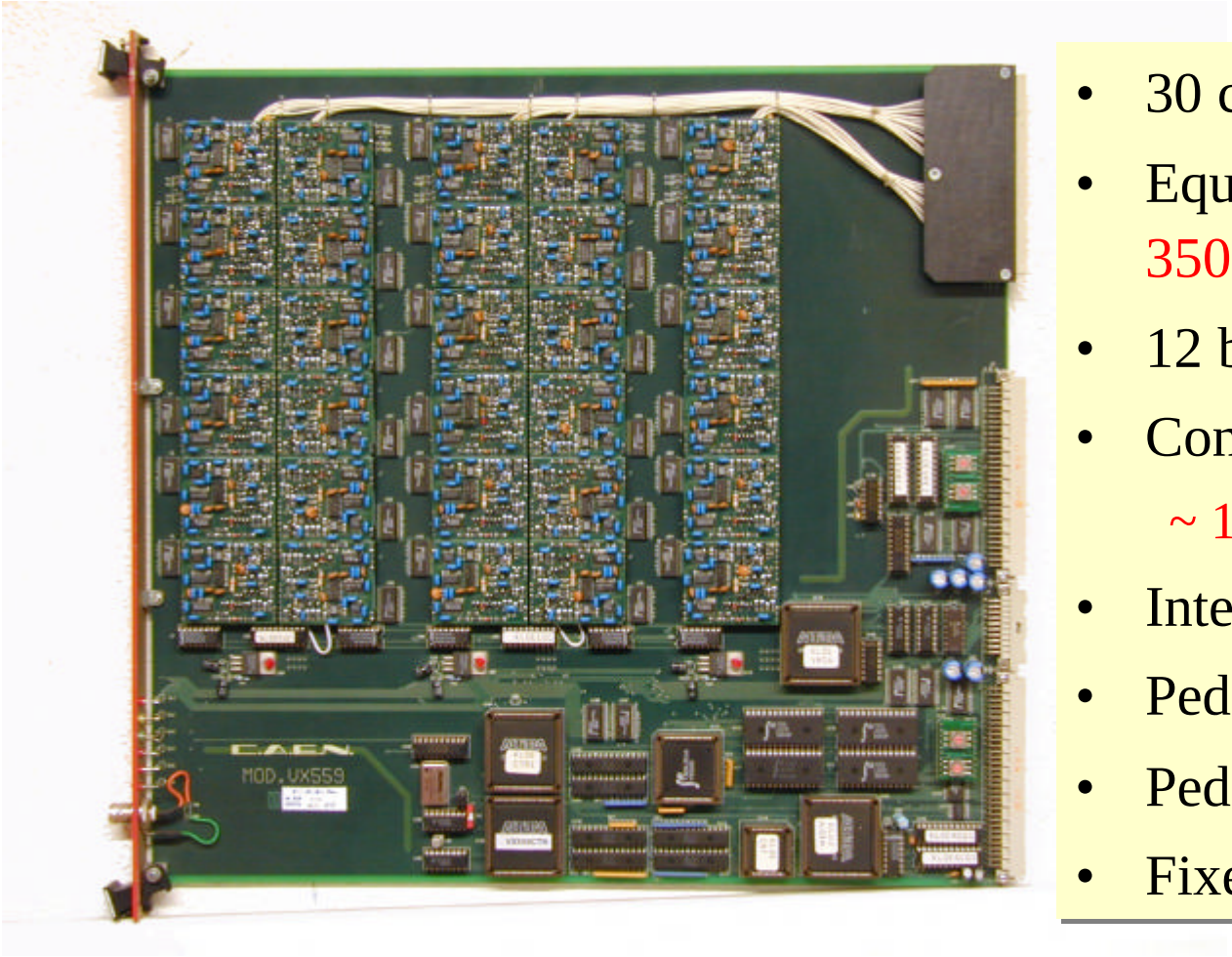
ADC working principle





- V/I converter
  - Match cable impedance with charge integrator input
    - Allow integrator long decay time
- Charge Integrator
  - Time constant ~ 0.5 ms
    - reduce sampling error
  - Cascode with FET input
    - Good bandwidth
    - Good linearity
    - Low noise
  - Bipolar output stage
    - capacitive load
- Sample and hold
  - 2 S&H free running with period of 900 ns
    - Guarantee correct baseline value in at least one S&H

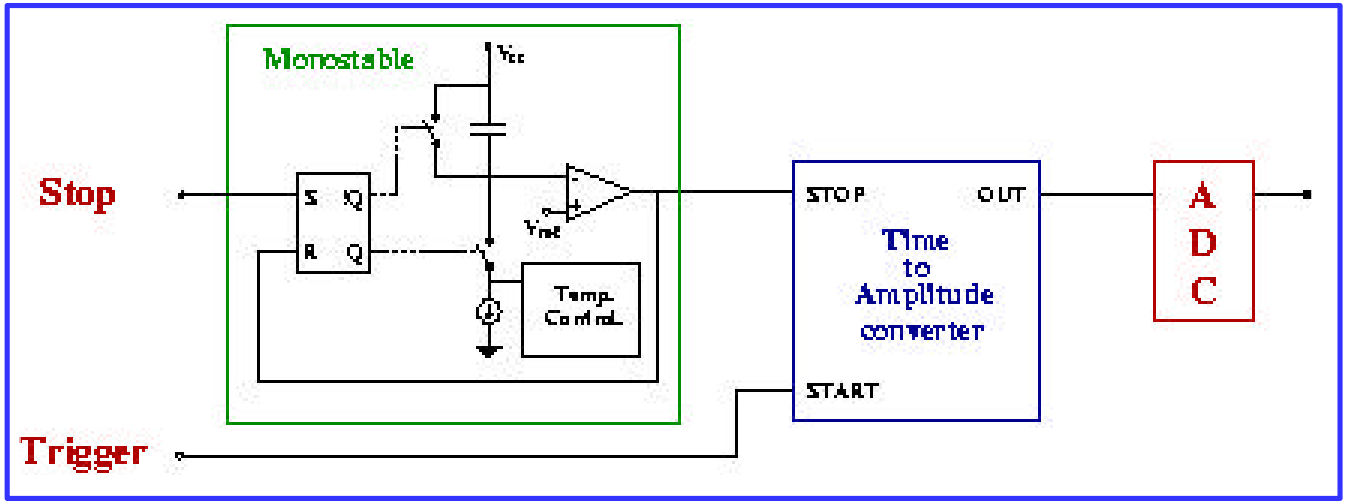
ADC performances



- 30 channels per board
- Equivalent gate ~ 200 ns (starting 350 ns before the trigger)
- 12 bit resolution
- Conversion gain

  ~ 100 fC/count (~ 0.2 MeV/count)
- Integral non-linearity < 0.3%
- Pedestal RMS < 1 count (0.2 p.e.)
- Pedestal and gain spread < ±3%
- Fixed conversion time ~ 2.3μs

TDC working principle



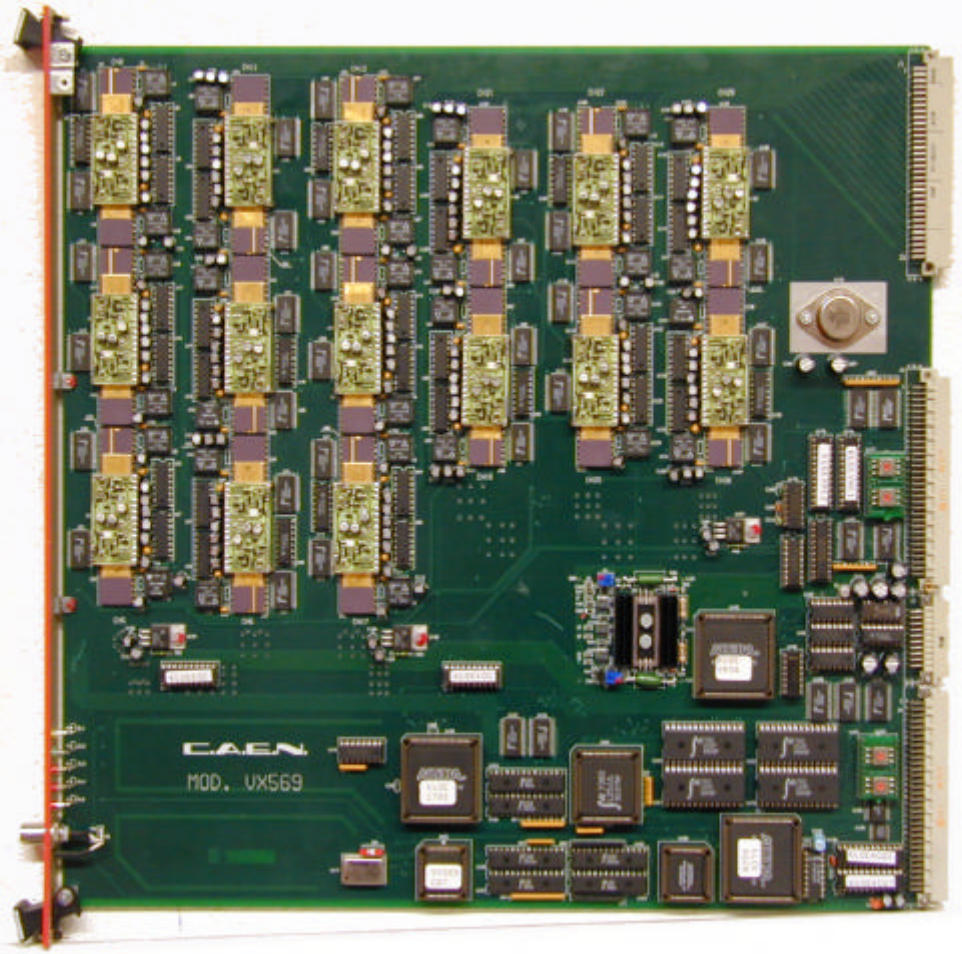
- TAC
  - Monolithic chip in bipolar technology
- Common start mode
  - Asynchronous trigger operation

- Monostable
  - Precise current source
  - Adjustable delay
  - Temperature compensation
    - trimmering system
    - monostable, TAC and ADC drift

TDC performances

- 30 channels per board
- 12 bit resolution
- Full scale 220 ns
- Conversion gain ~ 54 ps/count
- Resolution < 1 count
- Integral nonlinearity < 0.2%
- Temperature coefficient

  < ±0.3 count/°C
- Fixed conversion time ~ 2.3 μs



ADC - TDC logic

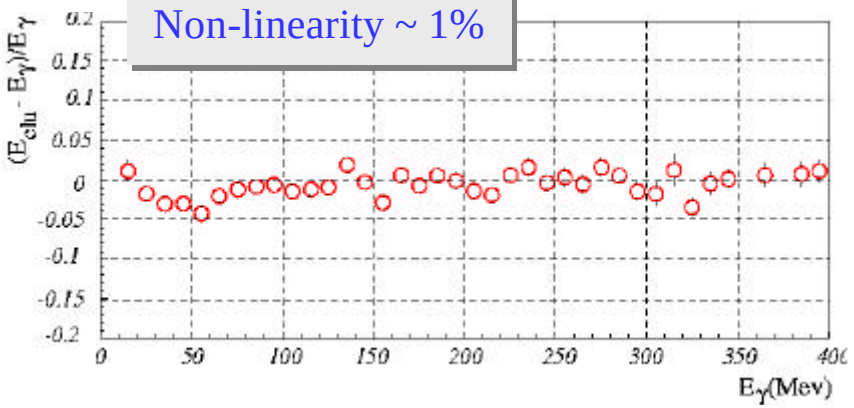
- Scan-logic
  - "Zero" suppression
    - Loadable look-up table
  - Pedestal subtraction
    - Loadable memory for ped. value
    - Hardware subtraction
  - Trigger counting
- VME -bus interface
  - Initialization
  - Monitor and test
- AUX -bus interface
  - Fast data read-out (40 Mbytes/sec)
  - Sparse data scan
  - Check trigger synchronization

- Two level hardware trigger
  - First level (T1)
    - Start ADC and TDC
    - Store data in latch
    - Fixed conversion time ~ 2.3 μs
      - ready to accept another T1
  - Second level (T2)
    - 2 μs after T1
    - Start data scan
      - Zero suppr. and ped. subtract.
    - Data buffering in FIFO
      - Channel number + data
      - Allow asynchronous read out

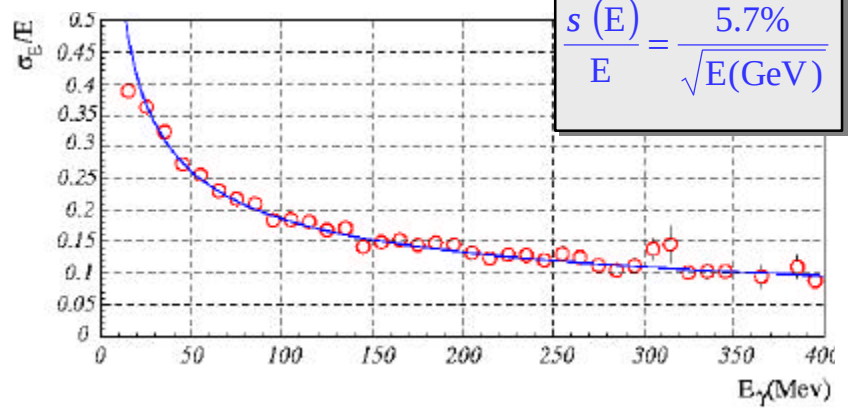
Energy performances

$e^+e^- \rightarrow e^+e^-g$ E_g from DC

Non-linearity ~ 1%



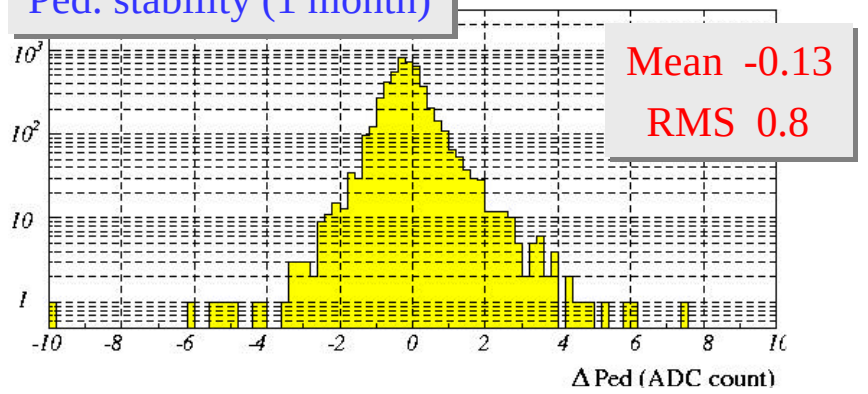
$$\frac{s(E)}{E} = \frac{5.7\%}{\sqrt{E(GeV)}}$$



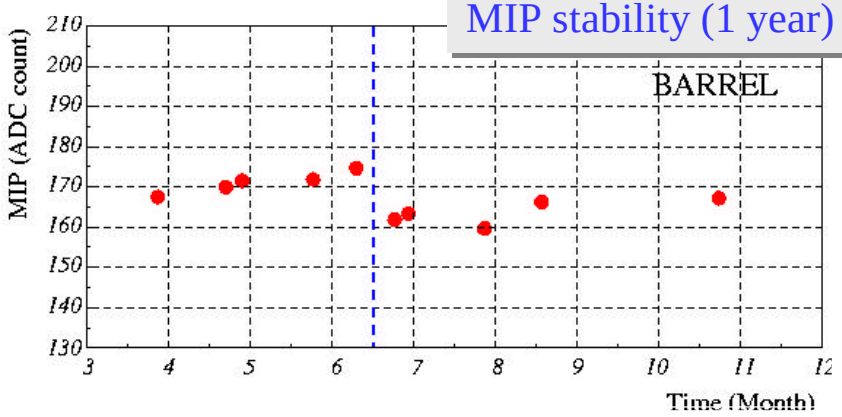
Typical pedestal rms 5 counts (1 p.e.)

Ped. stability (1 month)

Mean -0.13
RMS 0.8



MIP stability (1 year)

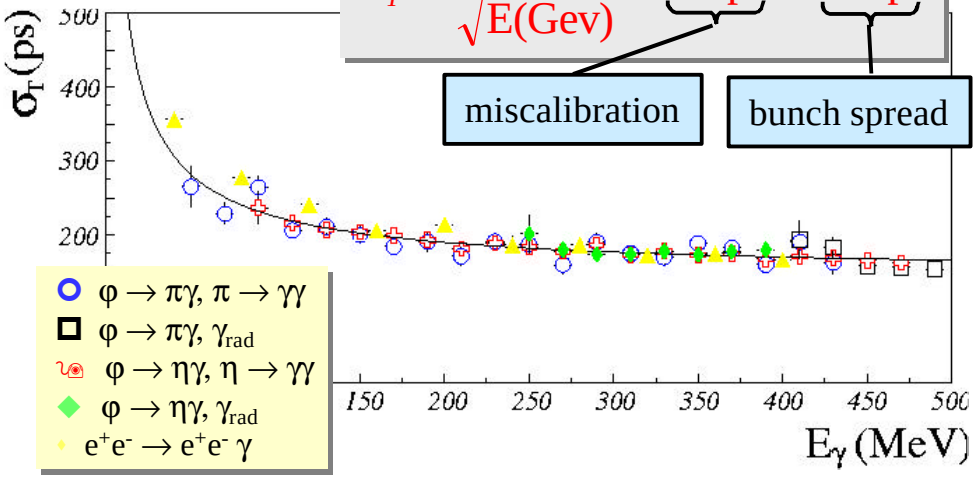


Time performances

$$\sigma_T = \frac{54\,ps}{\sqrt{E(Gev)}} \oplus 40\,ps \oplus 140\,ps$$

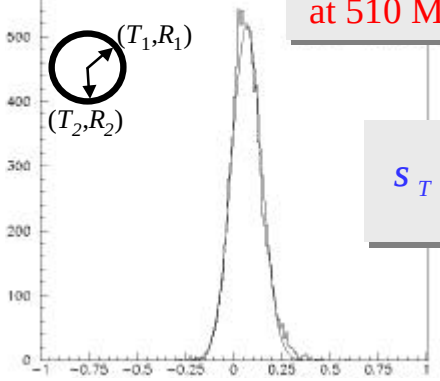
miscalibration

bunch spread



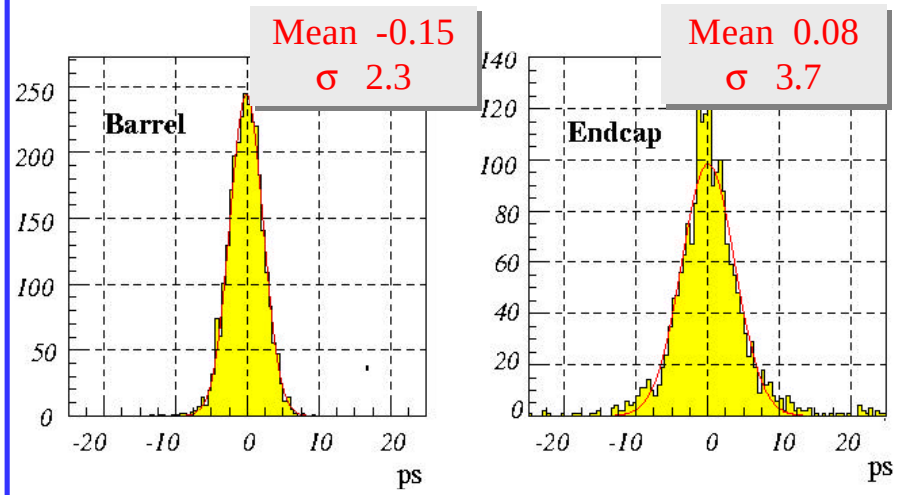
$e^+e^- \rightarrow gg$

σ_T = 110 ps at 510 MeV

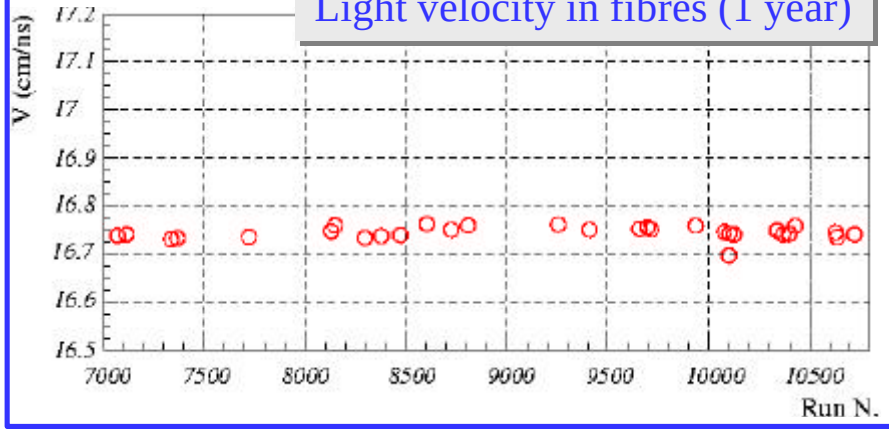


$$\sigma_T = \frac{70\,ps}{\sqrt{E(Gev)}}$$

T0 stability (1 month)



Light velocity in fibres (1 year)



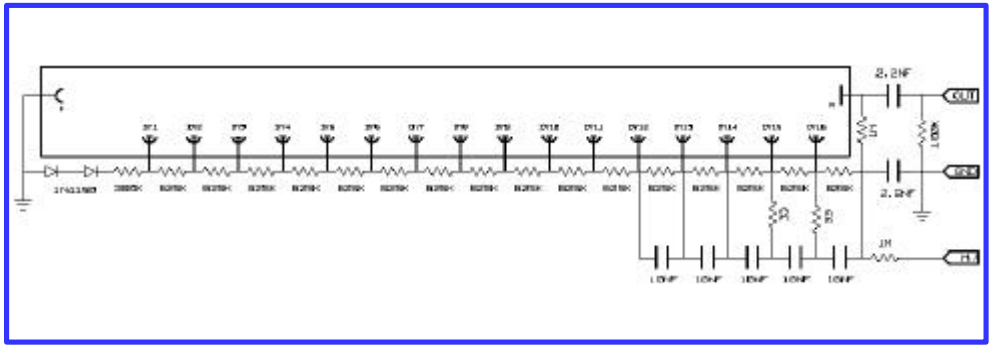
Conclusion

- **The KLOE calorimeter and its FEE have been kept in operation for more than 2 years**
- **The measured performances are in good agreement with the specifications**
  - **Energy resolution ~ 5.7% / ÖE(Gev)**
  - **Time resolution ~ 54 ps / ÖE(Gev) Å 40 ps**
  - **Good timing and energy stability**
- **Good reliability has been reached**
  - **0.1%** bad channel (preamp, SDS daughter board, ADC, TDC)

PM and HV divider

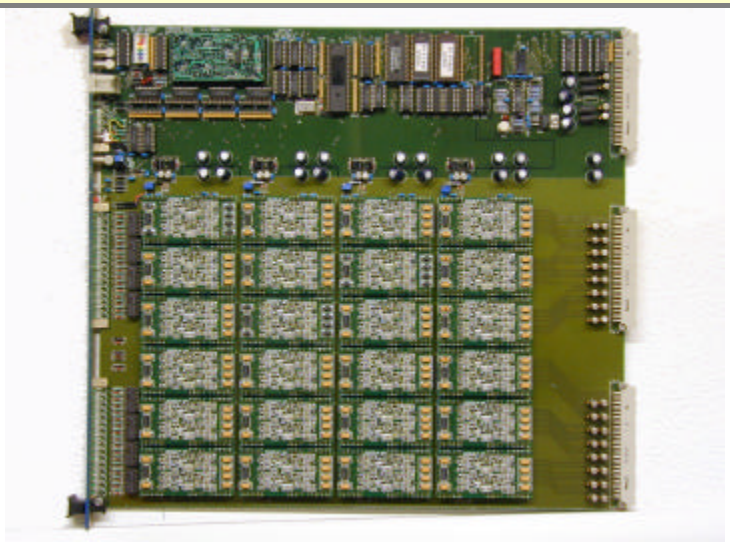
- Fine-Mesh type
  - Hamamatsu R5946/01 1.5′
    - 16 stages
    - Rise time < 1.9 ns
    - Transit time spread < 0.35 ns
    - Gain ~ 10^6 at 2000V
  - Magnetic field effect
    - 0.1-0.2 T with an angle < 25° respect PM axis
    - Gain change ~ 10%
    - No effect on linearity and resolution

- Grounded cathode scheme
  - Avoid noise due to micro-discharges
- Low current divider
  - ~ 150 μA at 2000 V
  - Low power dissipation
  - Self extinguishing at high light level



Control and Power

- Crate controller (16 SDS)
  - Custom crate bus for SDS control
    - Threshold downloading
    - Temperature and voltage monitor
  - Interface for remote access
    - H.S. CAENET and RS232
  - Pulse test generation
    - 96 pulser (5 PMs each)
    - 8 bit resolution



- Linear power supply (SDS+Preamp)
  - AC in 380V, 3 phases
  - Dual output voltages
    - ± 5V/54 A
    - ± 6V/50 A
  - Output power ~ 300 W
  - Shunt of two modules
  - Low output noise < 2 mV_{PP} (0 - 20MHz)