CALOR 2000

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The Front-End electronics for LHCb calorimeters

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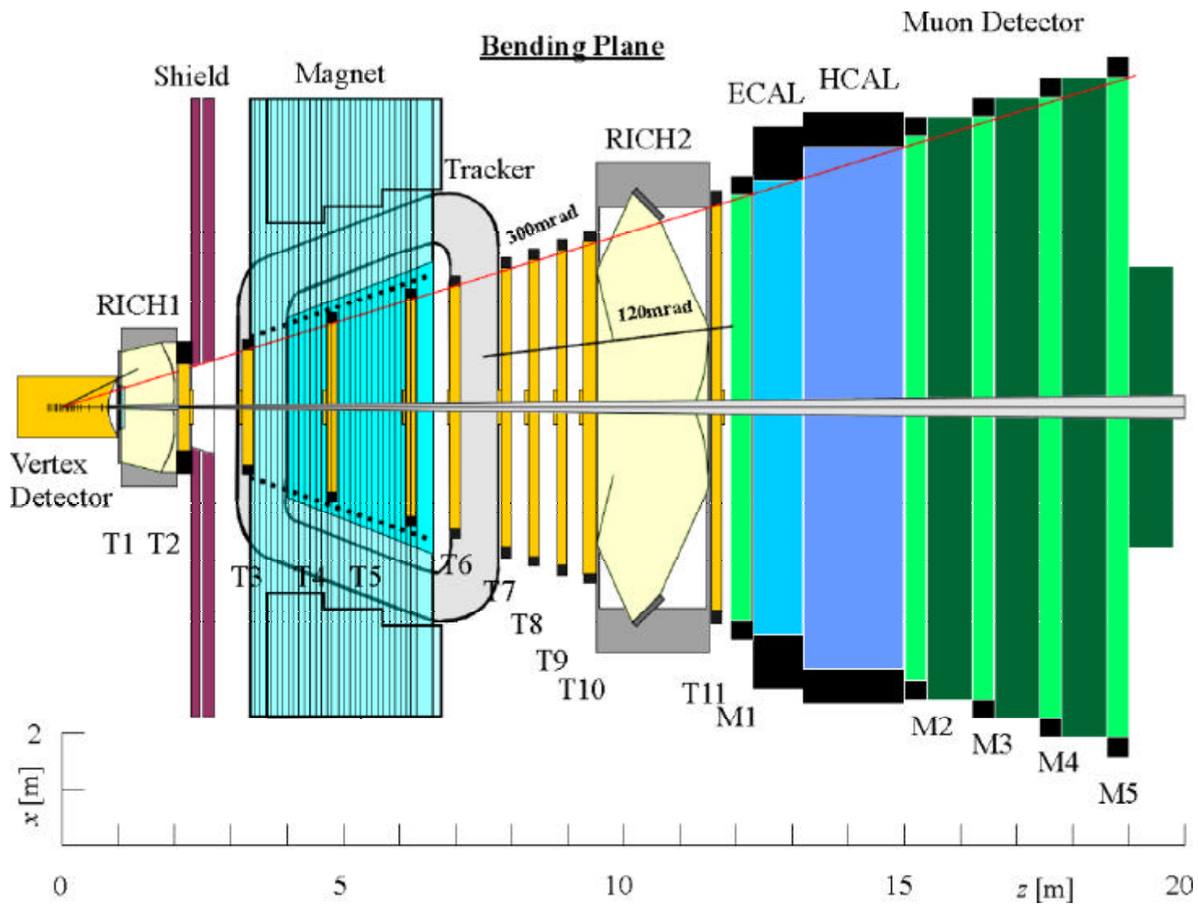
On behalf of the LHCb calorimeter team

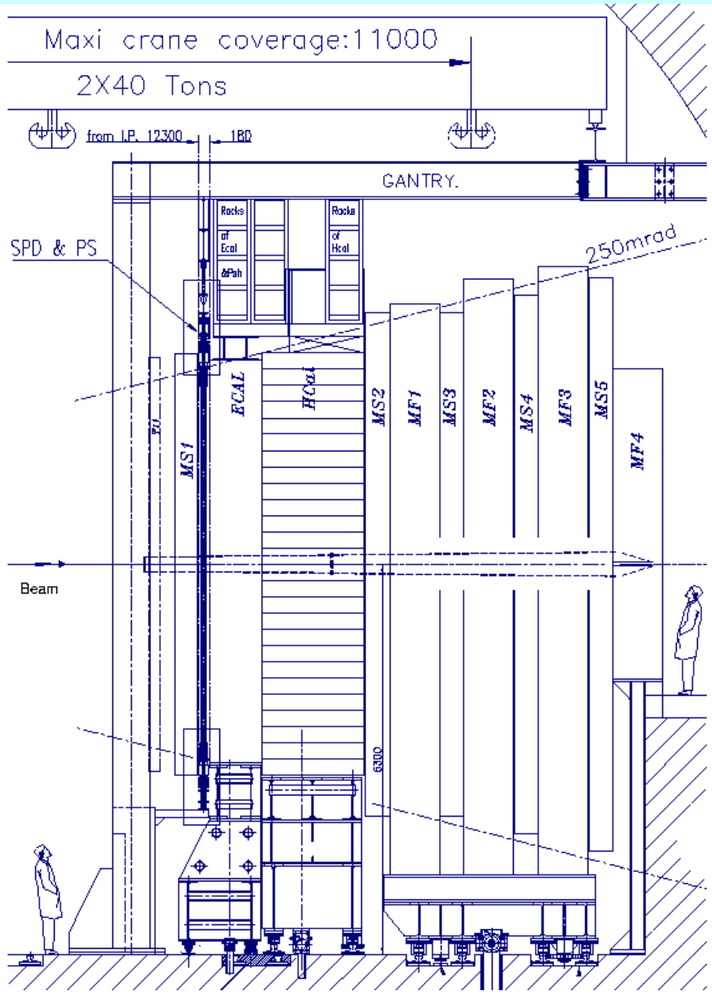
LHCb calorimeter main features

- The calorimeter system is used in several stages for Level 0 and Level 1 triggers and off-line analysis
  - Provide hadrons, photons and electrons candidates
    - Measurement of their energy and position .
      - Selectivity and fast response
  - Provide identification of photons
    - Good background rejection
      - Preshower detector
- High level0 rate , high occupancy
  - Full information every 25 ns
  - Level0 yes possible every 25 ns
- Cost/performance compromise.
    - Ecal based on Shashlik technology.
    - Scintillating tile geometry for the Hcal.
    - Common front-end electronics for Ecal and Hcal

The LHCb detector



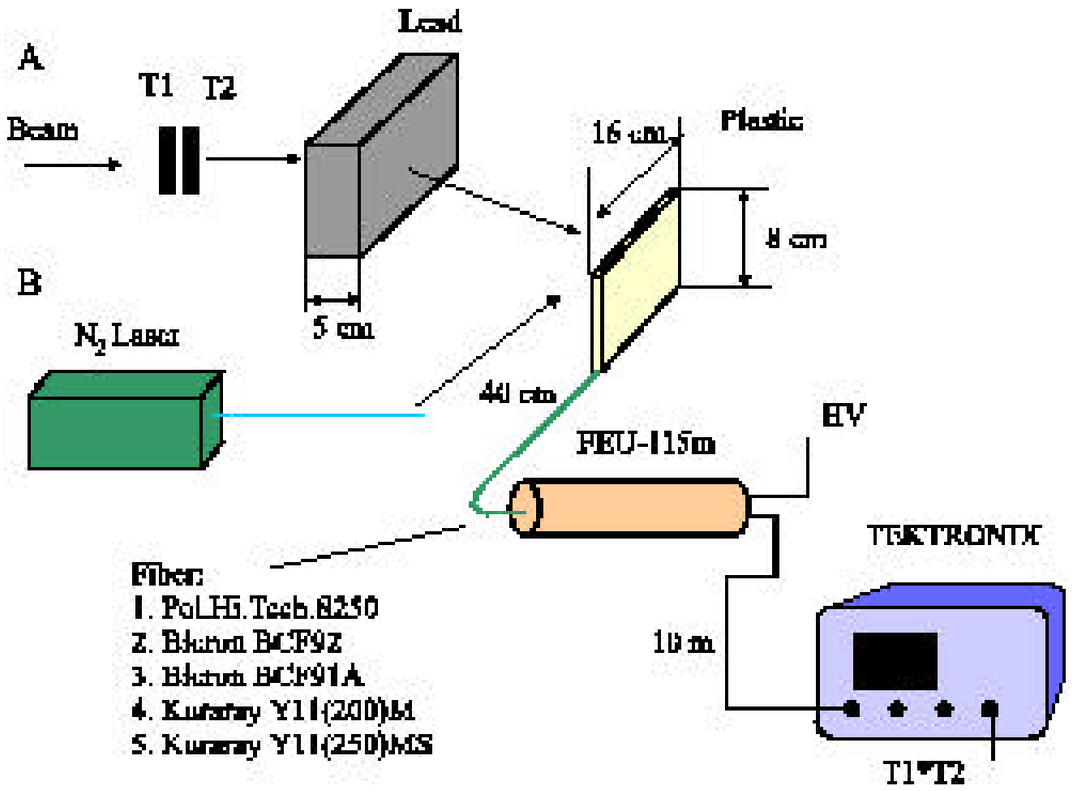
The LHCb calorimeters and muon chambers



Requirements for the calorimeter front-end electronics

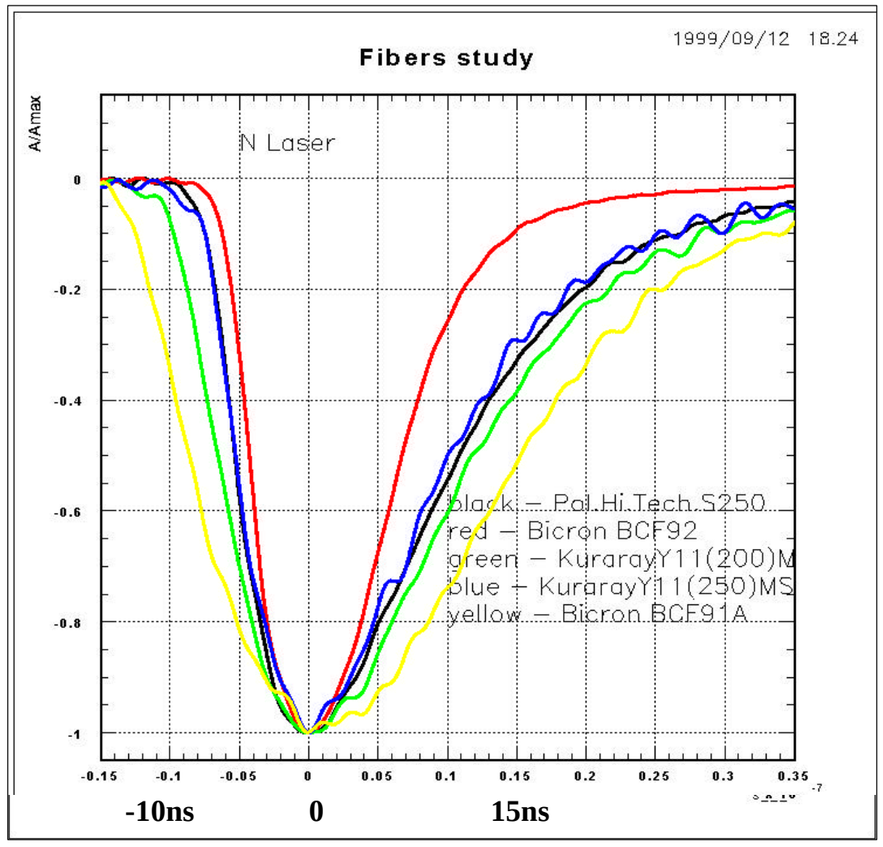
- Provide a fast signal :
  - Fast Pms covering the whole dynamic range of the 2 calorimeters
  - WLS Fibers with fast decay time
- Shape the input signals from PMs with total pile-up independence
- Perform analog to digital conversion on 12 bits at 40 MHz
- Perform a LF noise rejection
- Convert data into energy thanks to LUTs for trigger and readout
- Buffer data during the Level0 trigger latency
- Derandomize and buffer data during the Level1 trigger latency
- Perform a event formatting
- Look for local energy maxima over the channels
- Send the trigger information to the Trigger Validation Boards

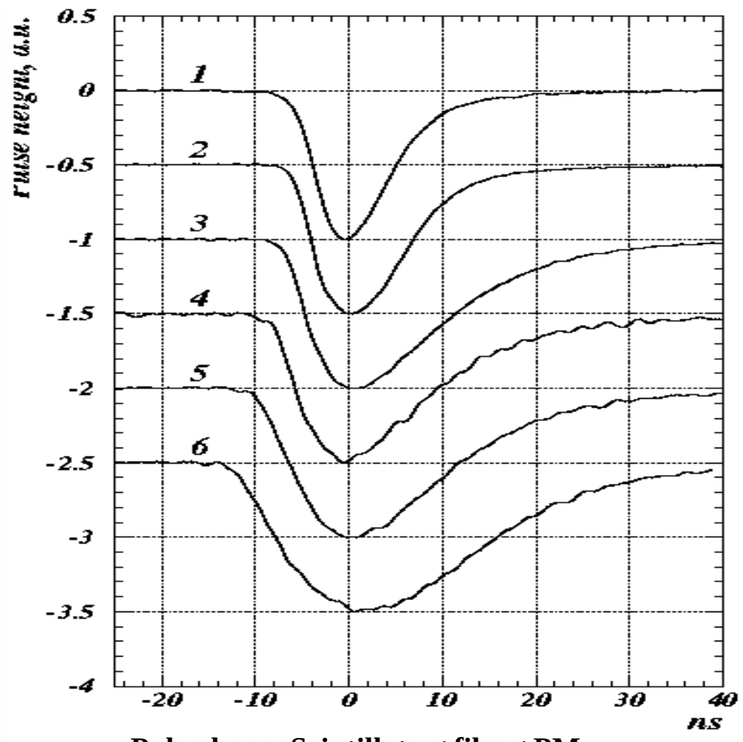
WLS fiber measurement setup



Measurement of the pulse shape properties using both X7 test beam and ultra violet N2 laser

Results of fiber study



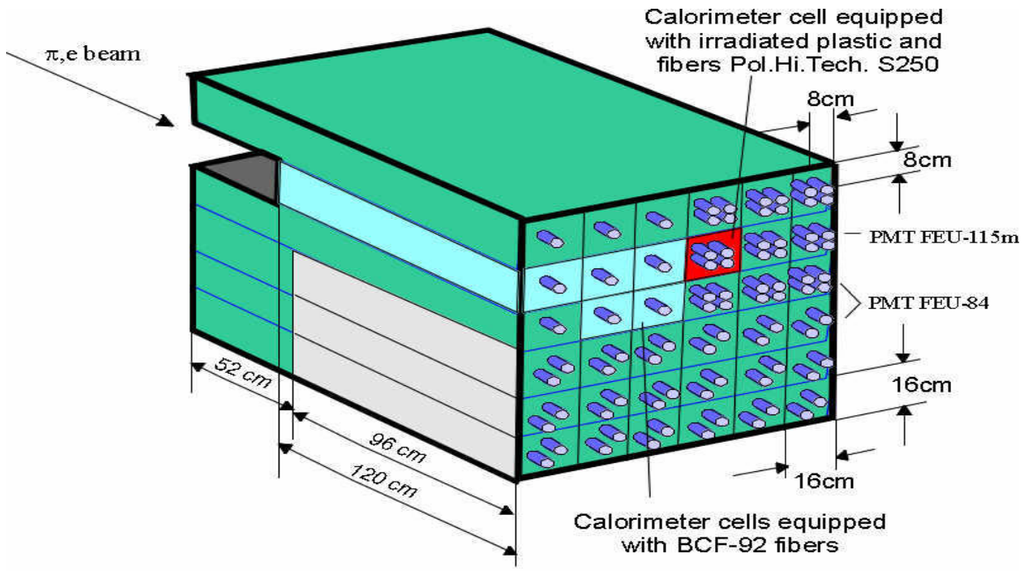


Pulseshape :Scintillator+fiber+PM

1 = BCF 92 Fibers

4 = Y11 fiber

Hcal prototype overview

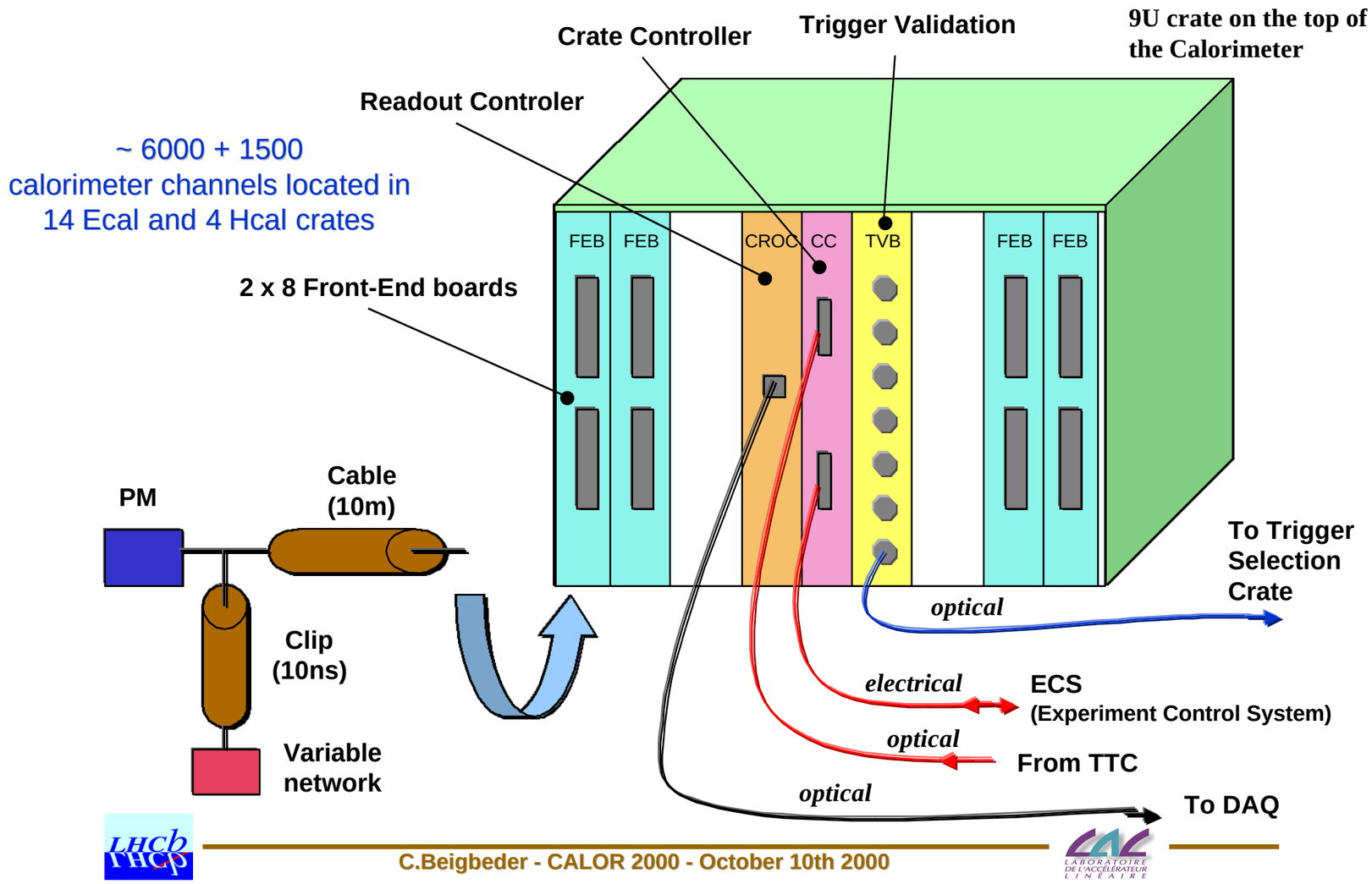


HCAL prototype

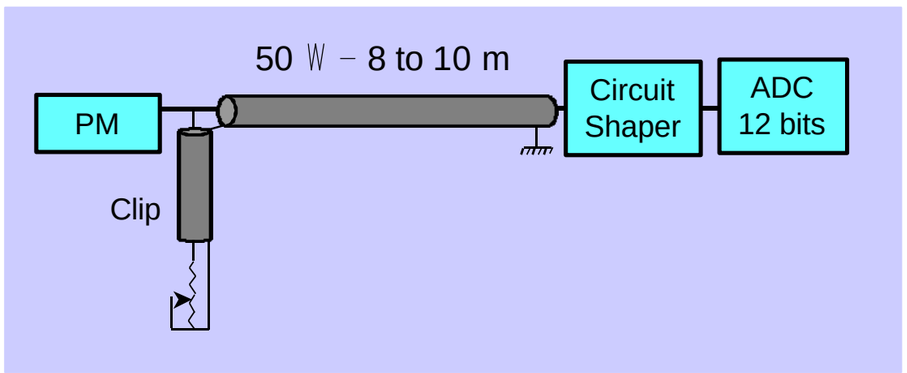
for 2000 tests

1. p/e beam; E, x, y, a - scan
2. HCAL performance with irradiated plastic (0.3 - 0.7MRad) and fibers (0.6MRad)
3. Signal shaping study fith fast BCF-92 fiber
4. Tests of FEU-115m-10 with new electronics
5. Combined tests with PS and ECAL

Front-End Electronics overview



Front_End elements

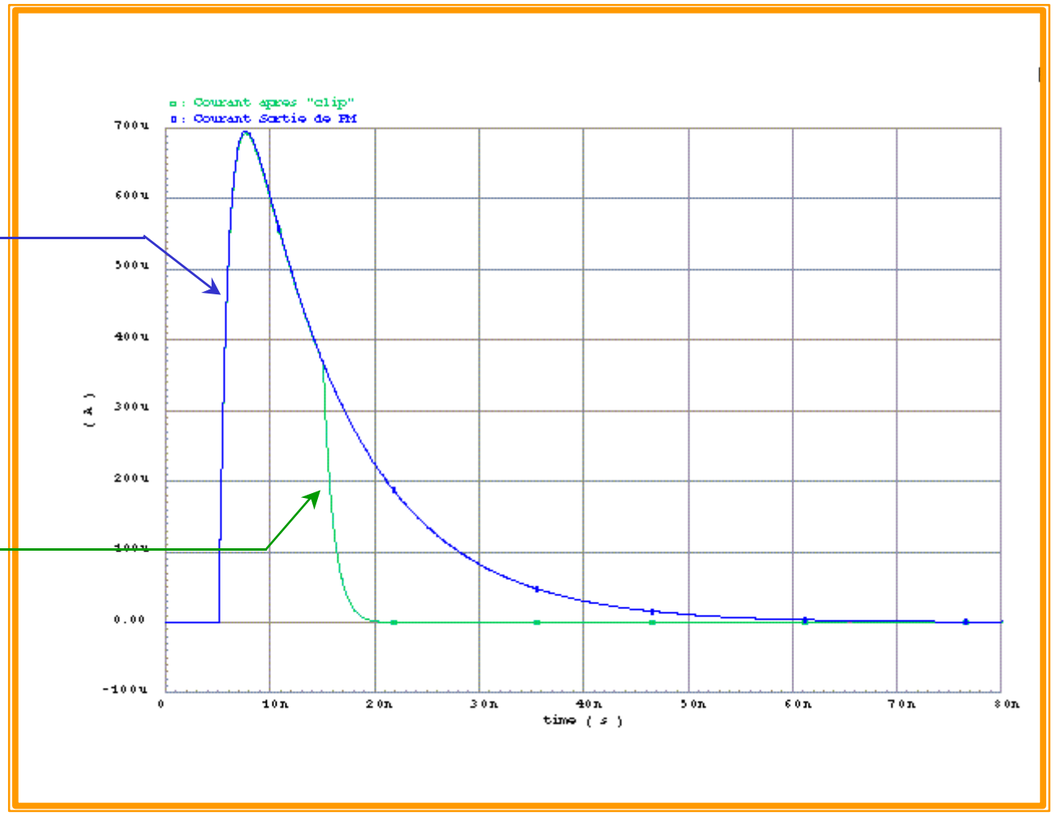


- Purpose :
  - To shape PM pulses in less than 25ns to avoid electronics pile-up.
- Specifications :
  - Input Signal 20mA over 25W
  - Dynamic Range : 1V at the input of the ADC (250 W)
  - Residue < 2% after 25ns.
  - Sampling with 1% precision over +/- 3ns after shaping.
  - RMS Noise < 1 ADC Count (i.e. 250 .v)

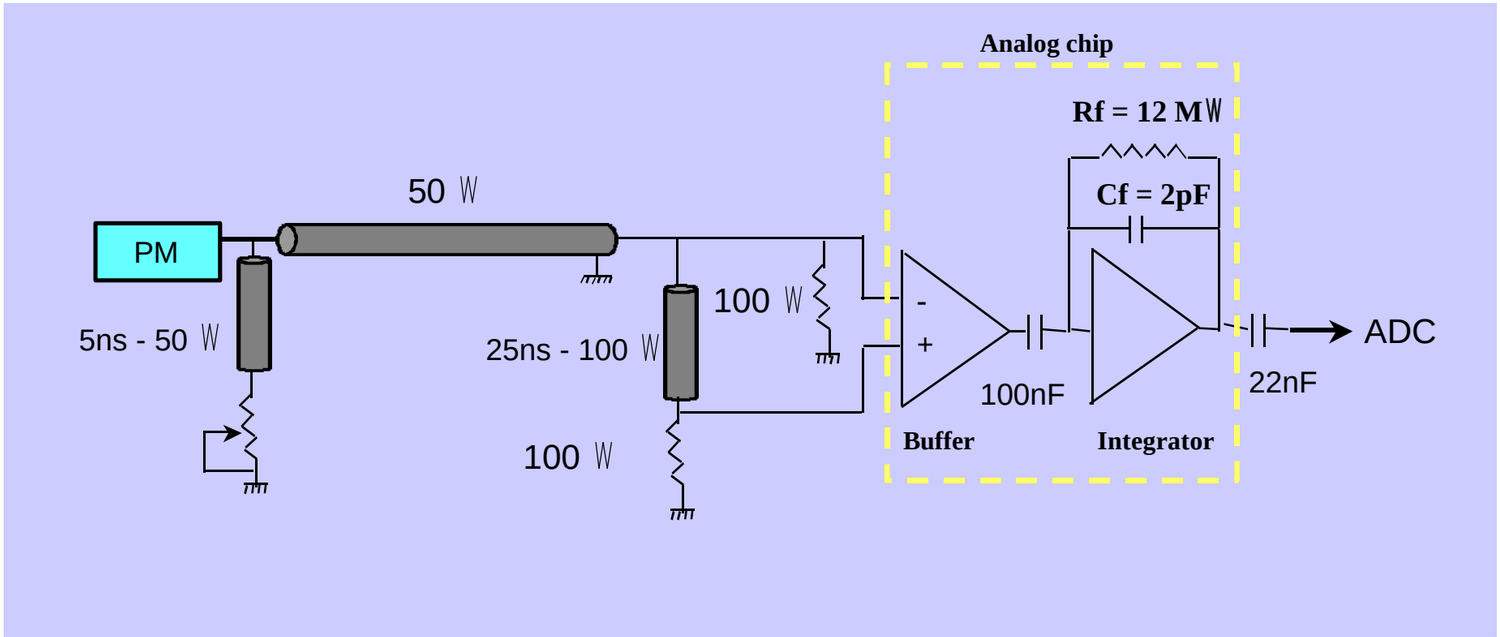
Simulated Input Signal

PM Output Current

Clipped Current



Principle of the Integrator Filter

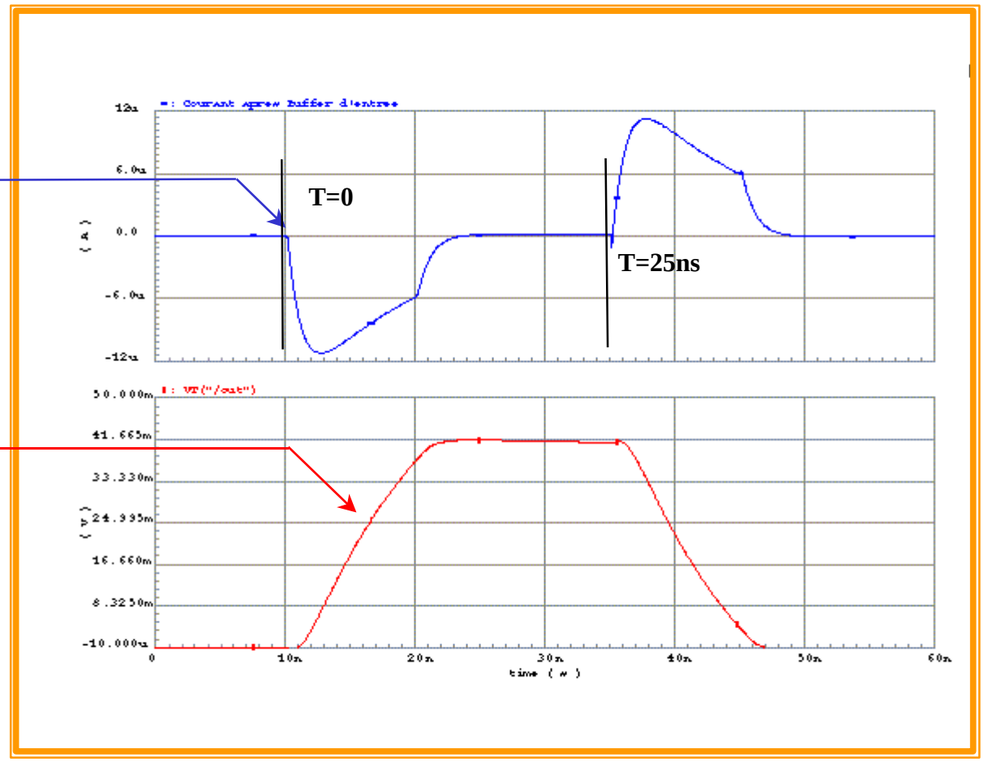


BiCMOS 0.8um ASIC
4 Channels per chip

Integrator Filter signals

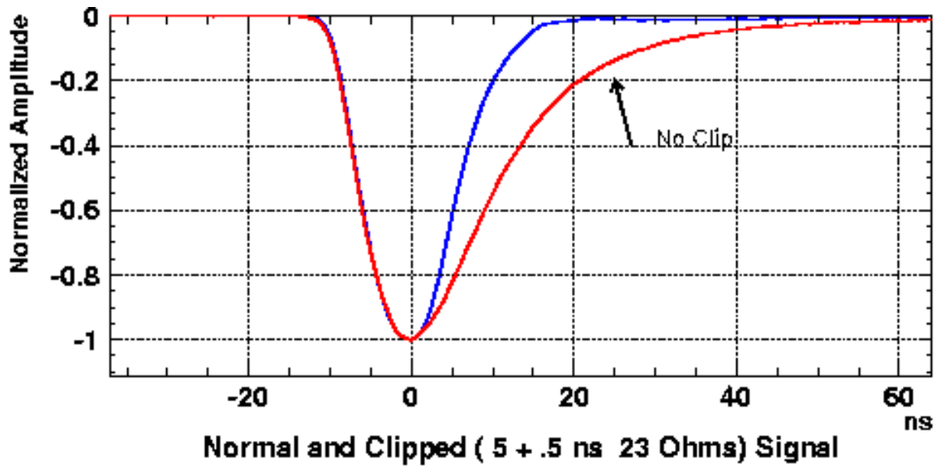
Buffer output current before integration

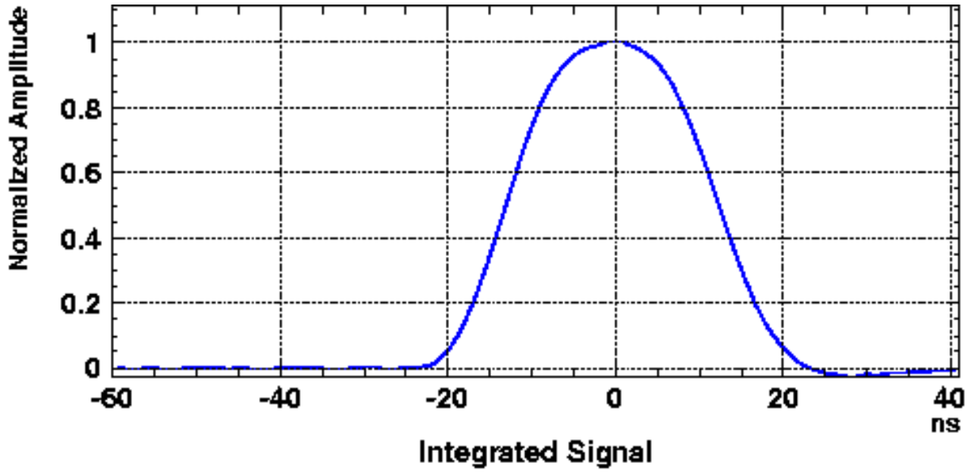
Output integrated signal



- Strobe on the flat top (» 10ns).
- Shaping : h(t) = [i(t) - i(t+25ns)] dt

PM input pulse and integrator output



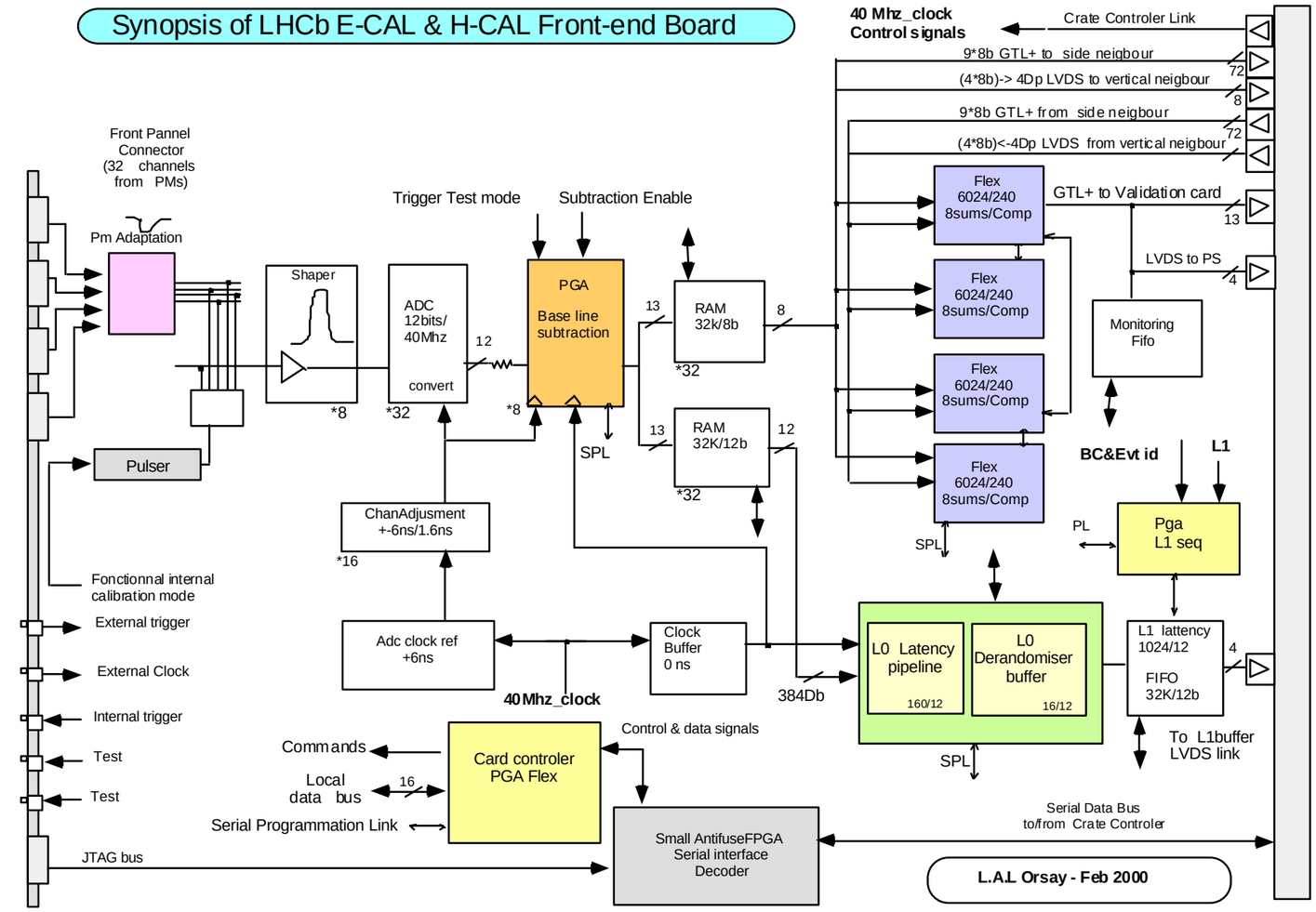


Both signals have been sampled by digital oscilloscope

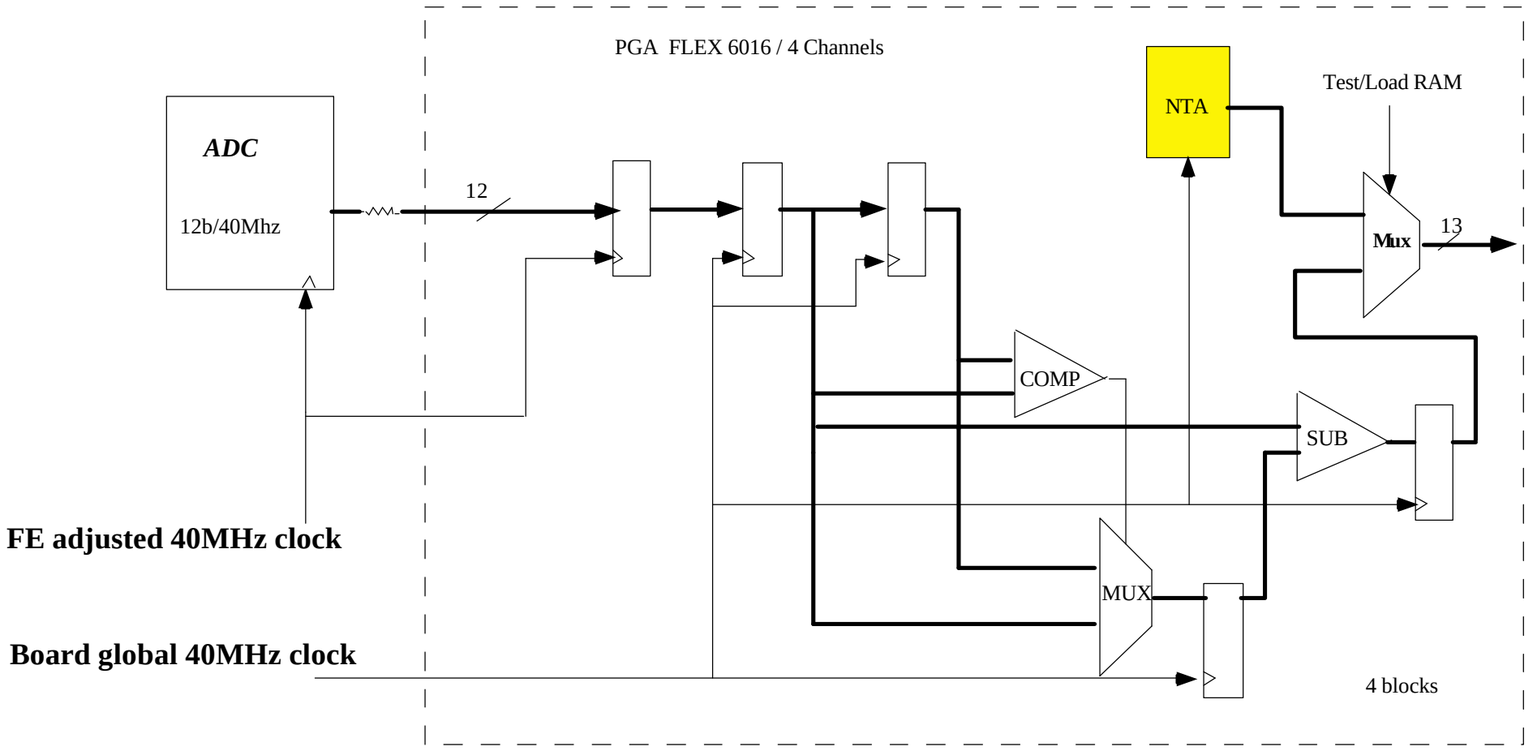
Integrator Filter performances on test bench

Simulation Results :			Current Test Bench Results :
Dynamic Range :	1.4V	<=>	1.4V
Non Linearity :	0.5%	<=>	<1%
Residue after 25 ns :	<0.5%	<=>	<1%
RMS Noise after subtraction 1 Adc count		<=>	1.1 Adc count
Power Consumption :	40mW / Channel	<=>	38mW / Channe
Open-Loop Gain :	~60dB	<=>	~60dB
gm (Input PMOS) =	34mA / V	<= >	18mA / V
Fall Time :	3us	<=>	2us
Rise Time (?) :	2.5ns	<=>	5ns
Input Impedance :	190Ω	<=>	270Ω

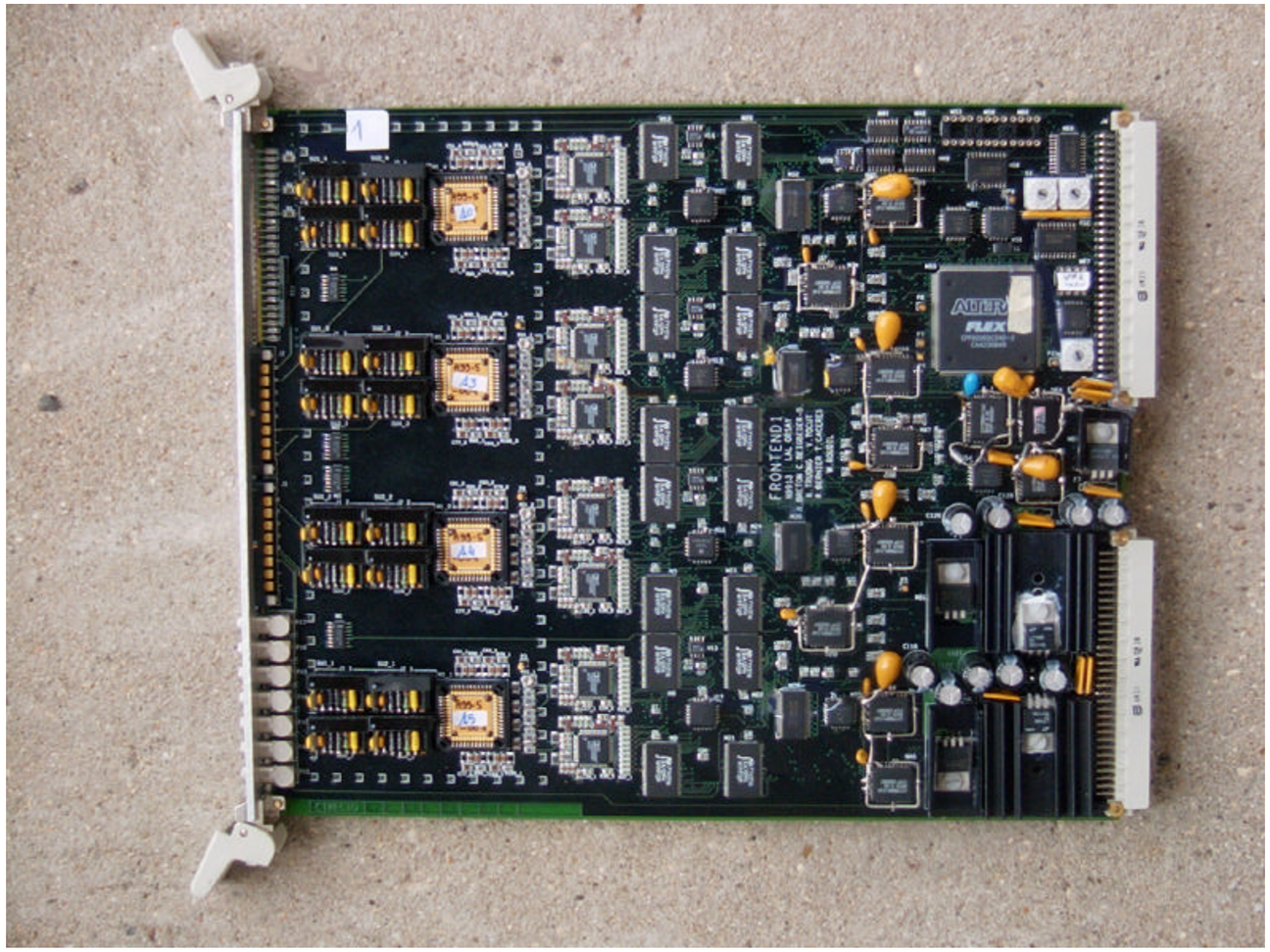
Block diagram of the Front-End Board



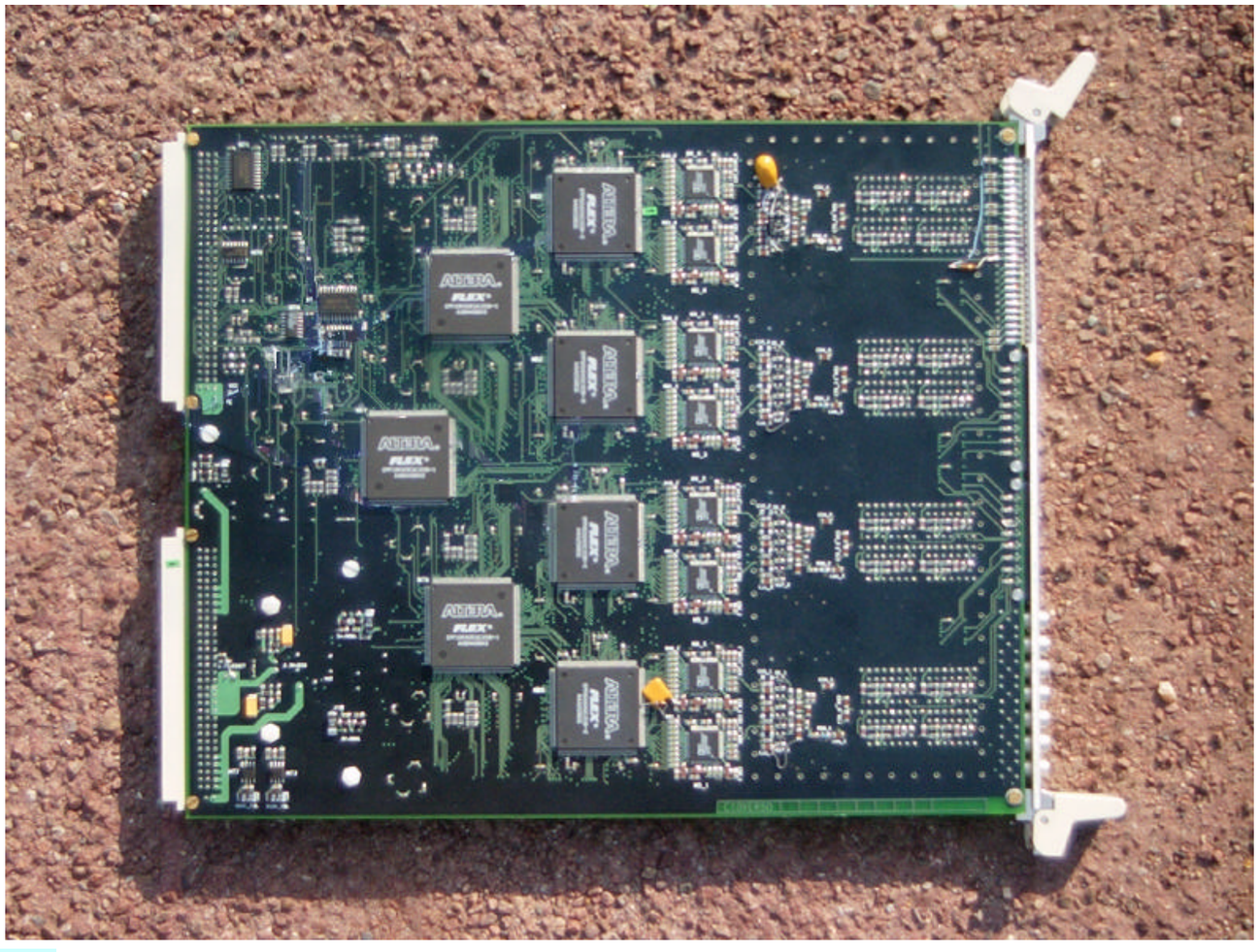
Block diagram of the baseline subtractor



Top view of the 16 channel prototype front-end board

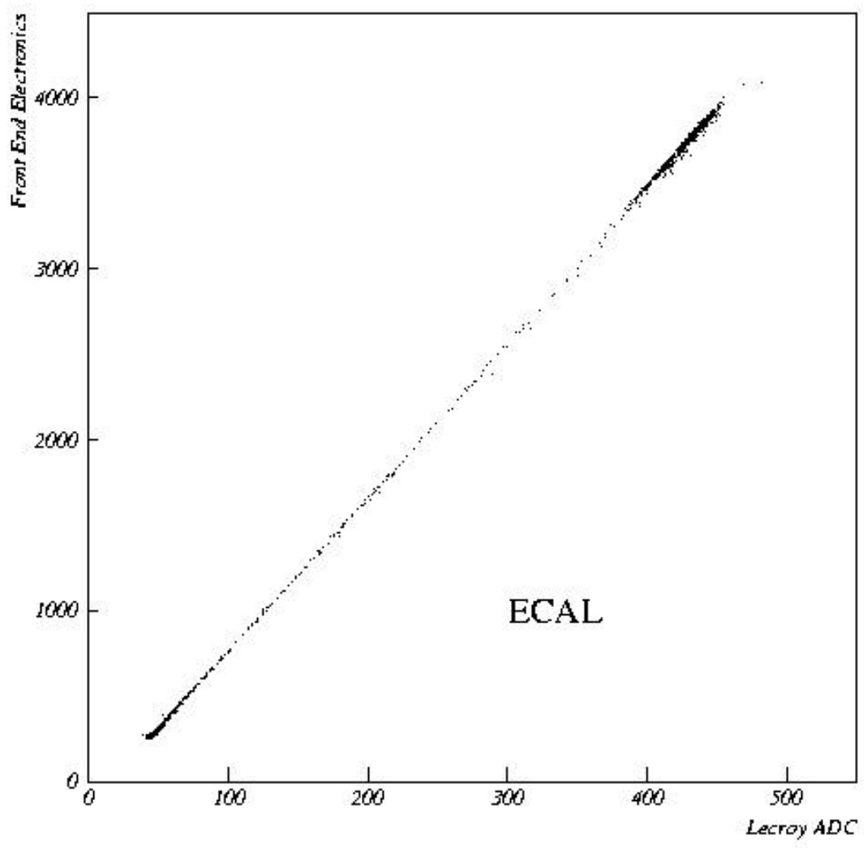


Bottom view of the 16 channel prototype front-end board



Front-end Board versus LeCroy ADCs

On this plot, one can compare 2 different types of readout channels for the same PM.

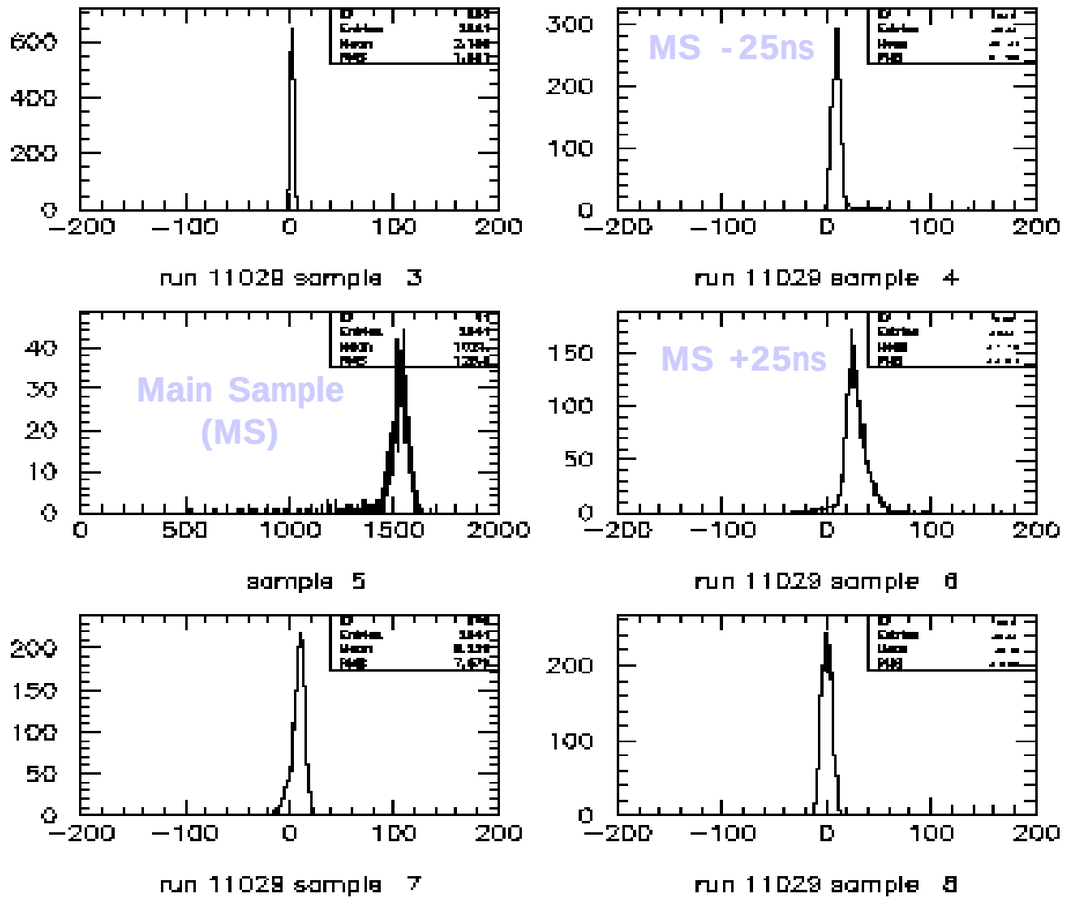


Test beam results

6 successive samples of ECAL pulses (samples=ADC measurements every 25 nsec)

Sample 5 contains the integrated charge information (note the different scale)

Other samples have contributions less than 2%



RMS Noise :

- **without subtraction (=> full integrator bandwidth) : ~ 20 adcc**
- **with subtraction : 1.1 adcc**

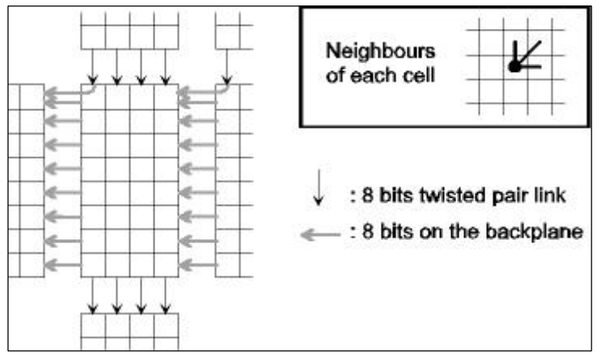
Trigger related operations on Front-End Board

- Operations on Front-End board
  - ADC data converted to 8 bits in a Look-Up Table (LUT)
    - Allows any coding. But should be additive
    - We foresee to use E_T coded on 8 bits, up to 5.12 GeV by .02 GeV steps
  - Data is sent to neighbors
    - on the card
    - via the backplane

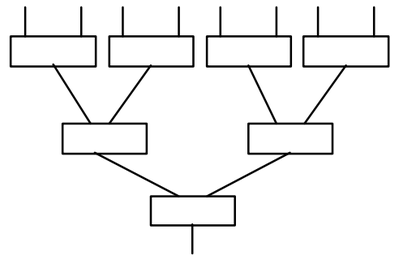
    => takes only one clock cycle.
    - or via short, serially multiplexed

    LVDS intercrate lines

    => could take more than one clock cycle.



  - Data is summed 2 by 2 in vertical lines
  - These sums are summed 2 by 2 in horizontal lines
  - The 32 sums (clusters) are compared and the highest one selected
    - Performed by a pyramid of "compare and select"
    - Should fit in 6 steps if the 45 energies enter the same big FPGA (~400I/O)
    - Currently fits in 10 steps within 4 “smaller” FPGAs
      - Confirmed by Verilog simulations
      - Could probably fit in 8 steps (under study)



Next steps of the developments

- Board design : Validation board (trigger concentrator), CROC (Crate and Readout Controller) and Backplane.
- Technical points :
  - Study on LVDS signals from 10MHz@100m to 280MHz@10m.
  - SEU problems :
    - More precise knowledge of the radiation environment required.
    - Board test setup for proton/neutron irradiation.