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VME Processor Evaluation

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CHANGE RECORD

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Approved by:		

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1. INTRODUCTION

This benchmark measure the Interrupt Response time and the Transfer Response time between an external VME memory module and the on board system memory.
The performance test is run over 10^8 samples. For each sample Interrupt and VME Transfer Response times are recorded. This test was run at the kernel level.
We are interested in verifying that the CPU board and the operating sytem can maintain their performance at **10 kHz** under heavy loading. All operating system facilities, such as TCP/IP and NFS networking are installed on the system under test.
The benchmark is performed using the **Digital Optical Link**[1] and **GPS satellite receiver BANCOMM bc637**[2] as VME target modules and is conducted with five asynchronous interrupting devices, wich include the real time clock, console, keyboard, network and external timer.

All of these measurements are made with PowerPC/LynxOS plateforms and the **VMTR2** board by **CETIA** is the reference board for this benchmark.

Manuf.	Board	Processor	Clock (Mhz)	DRAM (Mbytes)
CES	RTPC8067LK	PowerPC604	96	32
CETIA	CVME604	PowerPC604	100	64
CETIA	VMTR2A	PowerPC604	100	64
CETIA	VMTR2	PowerPC601	66	32

Table 1, Boards evaluated

2. INTERRUPT

2.1. Definition

The interrupt response time is the delay between the generation of the interrupt on the VMEbus and the execution of the corresponding interrupt routine.

2.2. Operating mode and results

We used as interrupt generator the **TIMING board**[3]**.** The response time was mesured using a **BANCOMM bc637 board**. The frequency pulse was set at 10kHz.

The results are given in figure 1.

[1] Digital Optical link board developed by **LAPP**
[2] bc637VME - **BANCOMM DIVISION** of **DATUM INC.** for more information see bc637VME/bc637VXI Operation and Technical Manual
[3] TIMING board developed by **LAPP**

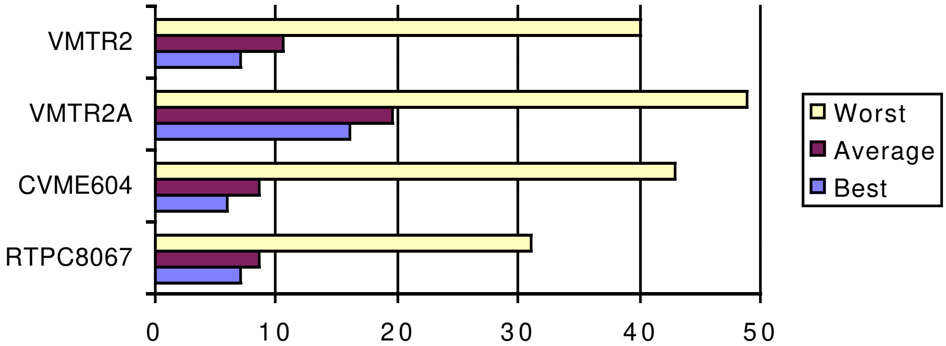

Figure 1, VME interrupt response time

(see also table 2 below)

µsecond	RTPC8067	CVME604	VMTR2A	VMTR2
BEST	7	6	15	7
AVERAGE	8.5	8.6	19.5	10.5
WORST	31	43	49	40

Table 2, VME interrupt response time

2.3. Obvervations

CES has changed the priority from VME interrupt to be served before all the other interrupts. CETIA has modified the real time clock interrupt routine and added kernel thread to handle this interrupt. The performance was improved, the worst case value was reduce from **61µs** to **43µs** (see table 2). This modification will be implement in next version of UNI/RT5[4]. Only the **RTPC8067** board was able to run at **10kHz** with original configuration. The **VMTR2/VMTR2A** board can not reach the aimed performance (≤ 6.2kHz).

3. VME SINGLE CYCLE

3.1. Definition

The VME single cycle response time is the time between two read/write cycles on theVMEbus, each cycle can have many VME single accesses.

3.2. Operating mode and results

We used the **BANCOMM bc637** board as VME target. Each cycle was composed of 3xD16 single access. The first read access to the internal register of the **BANCOMM bc637** latches the current time, the other read accesses read the time registers. The difference between the time in each cycle give the time for 4xD16 single access.

[4] UNI/RT5, LynxOS system provided by CETIA

The results are given in figure 2.

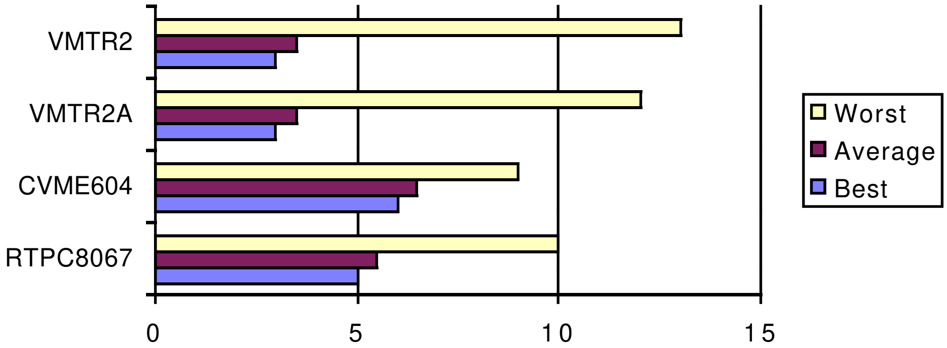

Figure 2, 4xD16 VMEbus single access response time

(see also table 3 below)

µsecond	RTPC8067	CVME604	VMTR2A	VMTR2
BEST	5	6	3	3
AVERAGE	5.5	6.5	3.5	3.5
WORST	10	9	12	13

Table 3, 4xD16 VMEbus single access response time

3.3. Observations

The difference between the **VMTR2/VMTR2A** board and the other platforms is due to the internal architecture. The **RTPC8067** and the **CVME604** boards use PCI bus and also the bridges ***(PowerPC ⇒ PCIbus, PCIbus ⇒ VMEbus)*** . This introduce a significant overhead.

4. VME BLOCK TRANSFER

4.1. Definition

The VME block transfer response time is the time taken by the VME block transfer function to setup and perform the VMEbus block transfer.

4.2. Operating mode and results

We used the **Digital Optical Link** board as VME source or target. The block transfer function was call in interrupt routine and so we must developed or modified existing source code to be used in kernel level.

The results are given in figure 3.

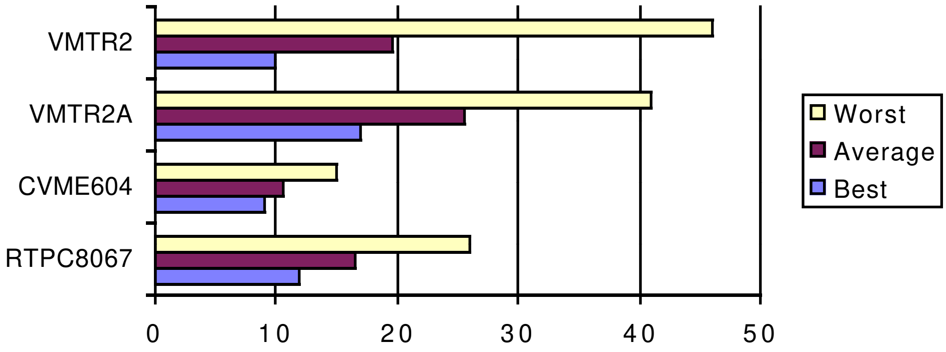

Figure3, 32xD32 VMEbus block transfer response time

(see also table 4 below)

µsecond	RTPC8067	CVME604	VMTR2A	VMTR2
BEST	12	9	17	10
AVERAGE	16.5	10.5	25.5	19.6
WORST	26	15	41	46

Table 4, 32xD32 VMEbus block transfer response time

4.3. Observations

CETIA has changed the write block transfer function. It did not used the DMA facility from the **UNIVERSE**[5] chip. This function was write in assembler code and used PowerPC facility to load and store the multiple instructions[6]. The performance was improved. The results are shown in Table 5. All the write block transfer waited on the End-of-Transfer flag , but we can work with *masked time* if we implement the DMA control.

µsecond	UNIVERSE DMA (READ/WRITE Block transfer)	CETIA FUNCTION (WRITE Block transfer)
BEST	5	9
AVERAGE	22.5	10.5
WORST	74.5	15

Table 5, CVME604 -VME block transfer performance

5. APPENDIX A - CHARACTERISTICS

[5] **UNIVERSE** PCI/VME bridge by **TUNDRA** for more information see Universe User manual
[6] **lmw and stmw**, PowerPC 60x assembler instructions for more information see PowerPC 604 RISC Microprocessor User's Manual

	RTPC8067LK	CVME604	VMTR2A	VMTR2
Manuf.	CES	CETIA	CETIA	CETIA
Processor	PowerPC 604	PowerPC 604	PowerPC 604	PowerPC 601
Clock (MHz)	96	100	100	66
DRAM (Mbytes)	32	64	64	32
L2 cache (Kbytes)	512	512	none	none
PPC/PCI	**IBM** 27-82660	MPC 105	none	none
PCI/VME	Owner	**TUNDRA** UNIVERSE	none	none
VSB	PMC **CES** VSB 8464	PMC **HEURIKON** PM/VSB	On board	On board
System	Full development	Full development	Full development	Diskless
LynxOS version	2.4.0	2.3.1	2.3.0	2.2.2

Table 6, VME processor characteristics

6. APPENDIX B - HISTOGRAMS

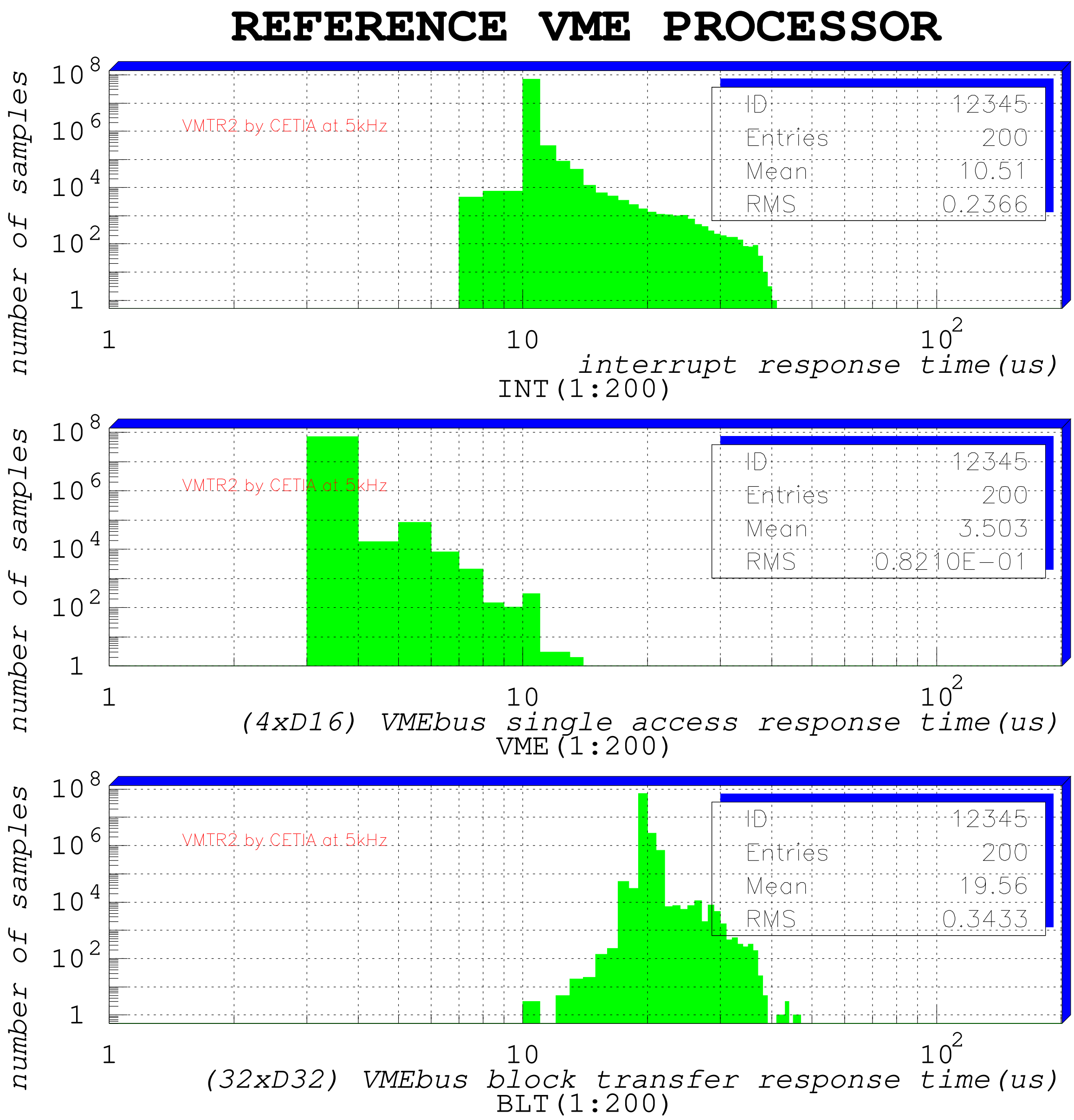

Figure 4, Reference VME processor performance

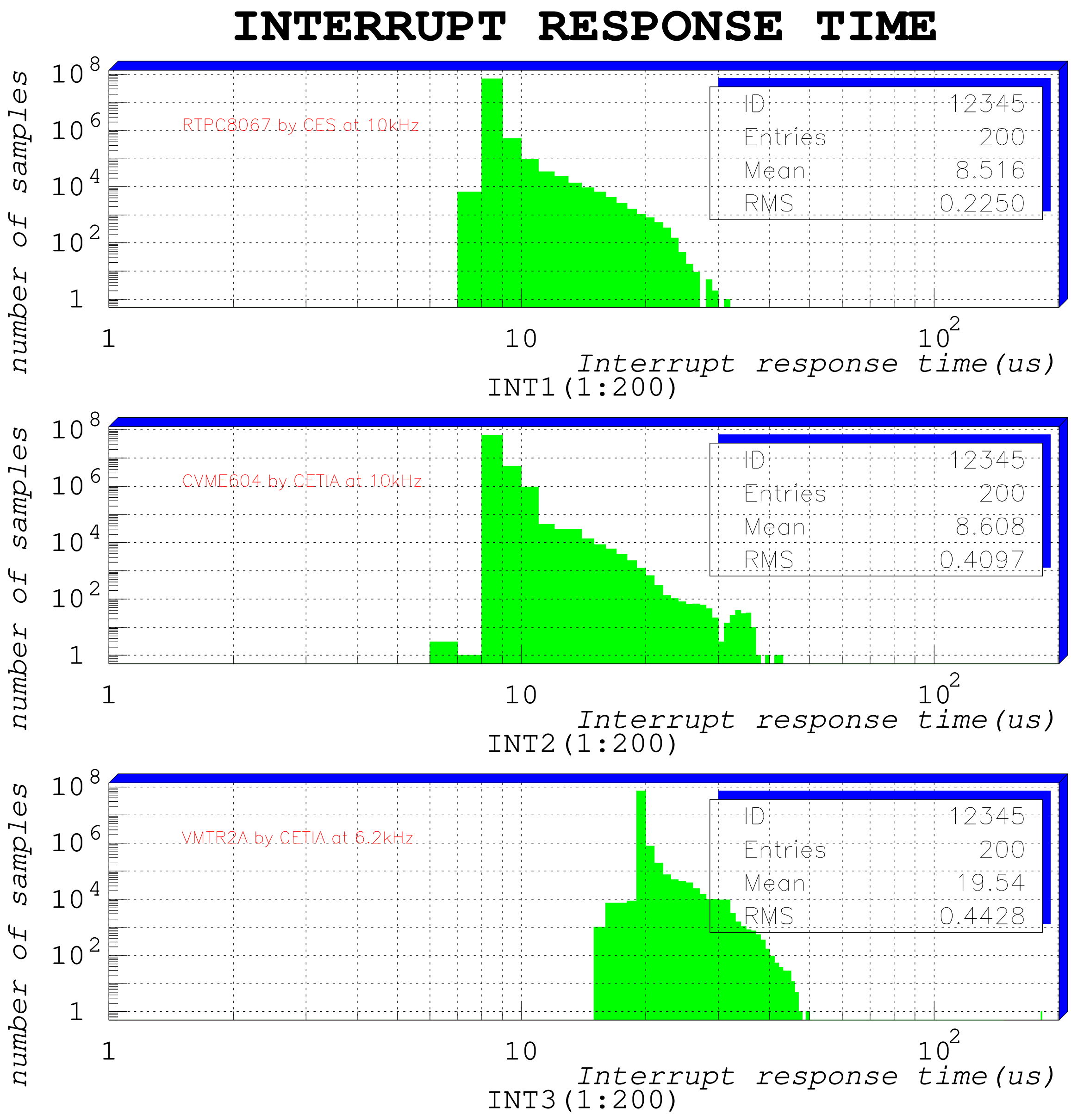

Figure 5, Interrupt response time

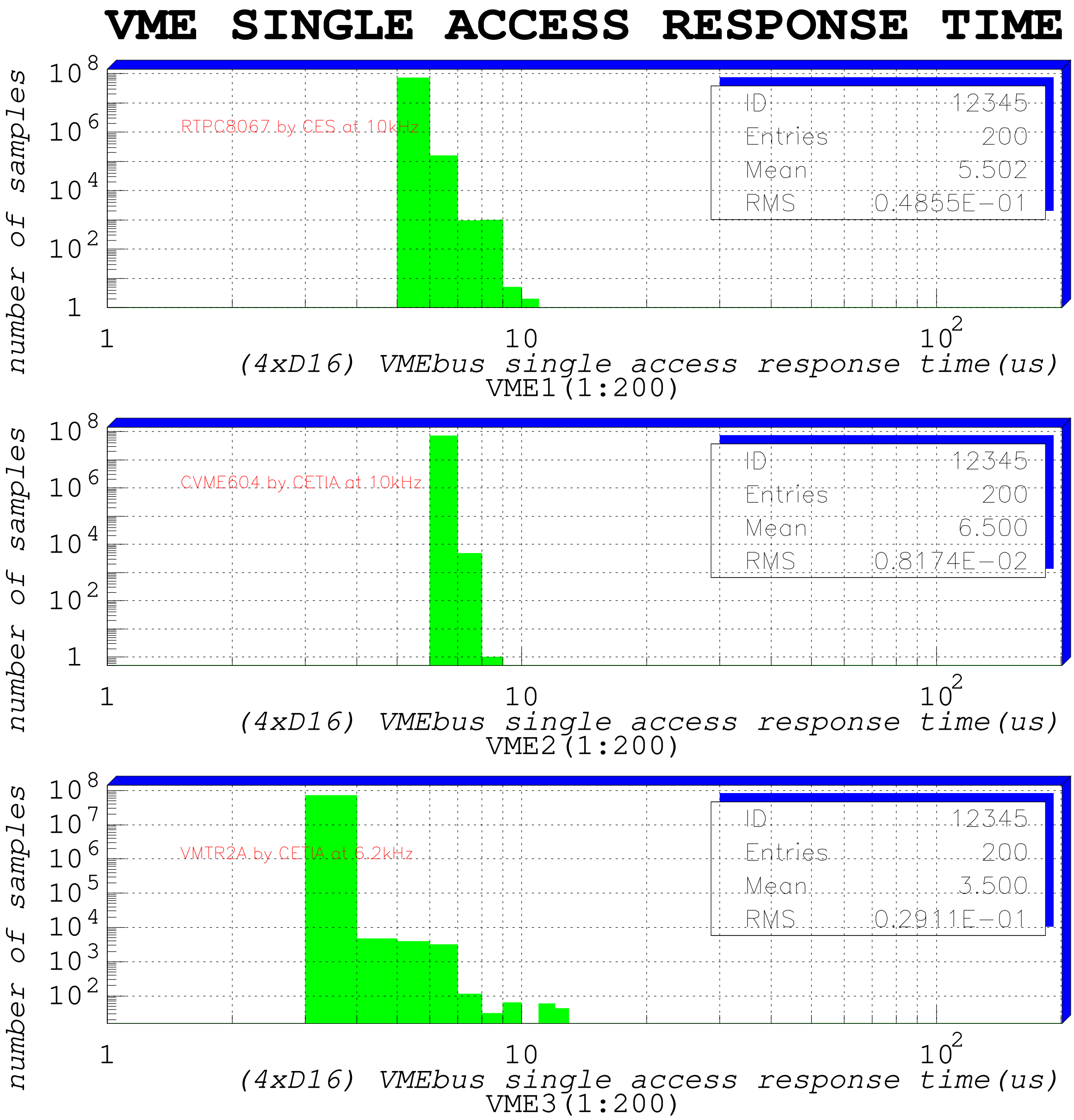

Figure 6, VME single access response time

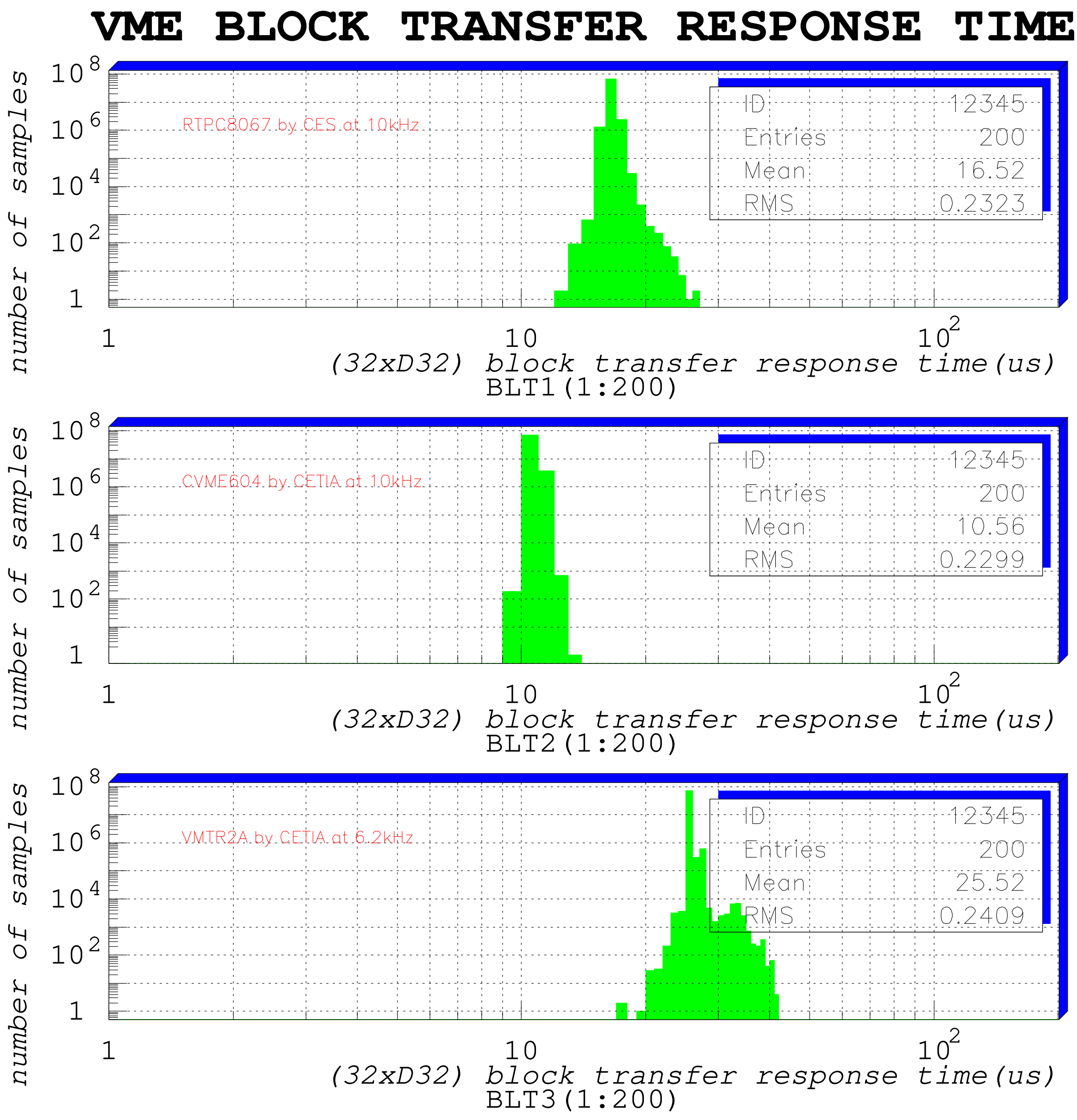

Figure 7, VME Block transfer response time