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Virgo ADC Selection and Tests Preliminary Results

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This note presents and justifies the preliminary choice of the main Virgo ADC boards, that will be used to acquire the dark fringe signal. A possible Mode Cleaner Control and Local Readout ADC board is also presented.

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1 Introduction

The interferometer output is the most delicate signal in Virgo. It's weakness, spectral shape and use in the interferometer locking require a very low noise acquisition. The Hamamatsu photodiodes output will be high pass filtered (in order to reduce the dynamic) and then read through ADC boards, whose performance in terms of effective bits has been fixed to 16.
Each photodiode gives 3 real current signals: phase, quadrature and DC. For 26 diodes these give 78 signals to read. So we need almost the same number of ADC channels, all with the required precision.

We need also ADC boards for the output bench control, and for the Local Readout System. Less strict requirements are needed for these, and consequently lower prices are imposed. We report also a series of preliminary tests made on one possible low cost board.

2 Dark Fringe ADC Boards

The requirements we put on the speed, dynamic and noise of such ADC are:

- Sampling frequency: $\geq 20\ KHz$;
- Readout frequency: $\geq 10\ KHz$, with block transfer capability;
- Input signal dynamic: $\pm 10\ V$;
- "True" ~ 16 Bits;
- White spectral noise $< 1\ \mu V_{rms}/\sqrt{Hz}$.

We have a VME based acquisition system, so we need boards made for such standard. Moreover, we want more than 78 channels, giving some limitations on their price.
A market evaluation selected the Etep (France) company in early '96; a prototype board was succesfully tested during the last summer. Then we ordered a first batch of 13 boards, and a full VME create was equipped with the final processor and low noise power supply. The boards assembled, models Etep 264A-265A, have 4 channels each and a total cost of 30000 FF for board (7500 FF for channel). The results we report have been made with this final configuration.

2.1 Technical Feature

Here are summed up the most important technical characteristics of the converters, as declared on the data sheet:

- Analogic-Digital converter: ADC5020 (Analogic Corporation);
- 18 Bits conversion;
- RMS Noise $\sim 60\ \mu V$;
- Conversion time: $\leq 5.0\ \mu s$;
- SNR: $\sim 100\ Db$.

The Etep ADC boards mod. 264A-265A have been designed for VME standard: the model 265A is a master, and propagate to the slave boards (mod. 264A) the VME access to each buffer. A maximum of 8 boards can be connected through a specific bus (P2): it distributes the clock signals, the feeds and readout of the buffers.
A review of the technical feature and connections are listed below:

- 4 channels each board;
- Input signal range $\pm 10\ V$ (or $\pm 5\ V$ commutable by switch);
- Conversion time $\sim 7\ \mu s$;
- Maximum sampling frequency $\sim 140\ KHz$;
- 16 most significative Bits exploited;
- Additional Kapton cable (P2), connecting 8 boards;
- Independent low noise power supply $\pm 15\ V$ and $\pm 5\ V$ (on P2 connector);
- External trigger (sampling and readout signals), propagating via P2;
- 32 bits data format (two 16 bits channel data each 32 bits word);
- Two FIFO buffers, 4K-bytes each (max 512 data for channel), changing (flip/flop) with the acquisition pulses;
- Digital board mod. Etep 265A (implemented only on the master board), managing the readout from 4 to 32 channels, through the specific bus P2, with block transfer procedure.

The clock signals are provided by a Timing VME board; they are TTL signals, of $10\mu s$ duration, synchronized, at two different frequencies generated from the division of a unique 100 KHz signal. The timing board generates also the VME interrupts with the acquisition signal.

3 Tests

3.1 Background noise

In the following we'll name background noise the sum of:

- fluctuations in the ADC zero level;
- errors in volts comparison;
- electronic noise;
- disturbs induced by board access and readout.

We can measure such noise without input signal. Our tests have been made with:

- Analogic inputs closed on 50 Ω;
- ADC input range: $A = \pm 10\ V$;
- 8 board (32 channels) readout;
- Sampling frequency: $F_s = 20\ KHz$;
- Flip/Flop (readout) frequency: $F_f = 10\ KHz$;
- Time of measure 3.5 s (70000 data);
- Analysis on 65536 points;
- FFT on 8192 points (bin width 2.44 Hz);
- 8 spectral averages;
- Rectangular window;

The spectrum is symmetric respect to half the sampling frequency. So the relation between the Power Spectral Density (S_{xx} , measured in $\frac{V_{rms}^2}{Hz}$) and ${\sigma_x}^2$ $[V_{rms}^2]$ is defined as:

$$ {\sigma_x}^2 = \int_0^{F_s/2} S_{xx}(\nu) d\nu \tag{1} $$

valid for a variable x with zero mean. Otherwise we would find the squared mean value added on the left side of eq. (1), and added at frequency 0 (first bin) in the Power Spectrum.
Another way to express the noise is the number of "effective bits"; this is the number of bits of an ideal (with only quantization noise) ADC that present the measured level of noise. This number can be deduced from:

$$ N_{eff} = log_2 \left(\frac{2A}{\sqrt{12}\sqrt{Fs/2}\sqrt{\overline{S_{xx}}}} \right) \tag{2} $$

In the pictures below are shown some typical amplitude spectra obtained with these ADC's.

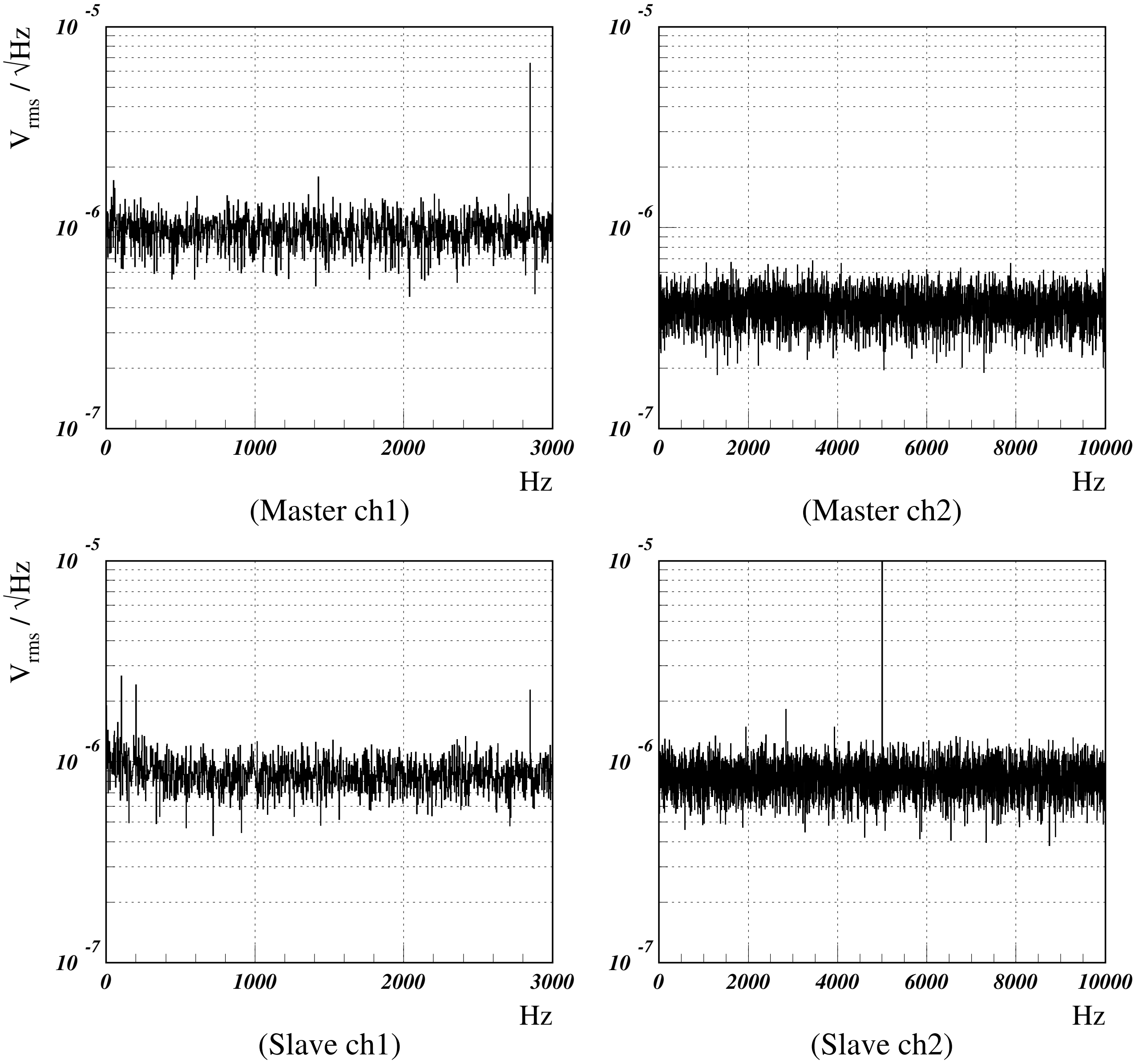

Figure 1: Up, amplitude spectra and low frequency zoom of the first two channels of a master board; down, the same for a slave board.

The noise is white excepted for unknown peaks at $\sim 1420\ Hz$ and its double on the Master, and for peaks at $5\ kHz$ (half the readout frequency) on the slave.
We summarize in fig. 2 the measures for all the channels of 8 boards in a dedicated VME create. The mean value of the background noise is $0.98\ \mu V_{rms}/\sqrt{Hz}$ or $15.84\ Bits_{eff}$: this value is close to the requirements, but some readout errors are still present (channels 10,19,29 in fig. 2, not included in the mean value). The nature of such errors is actually under study.

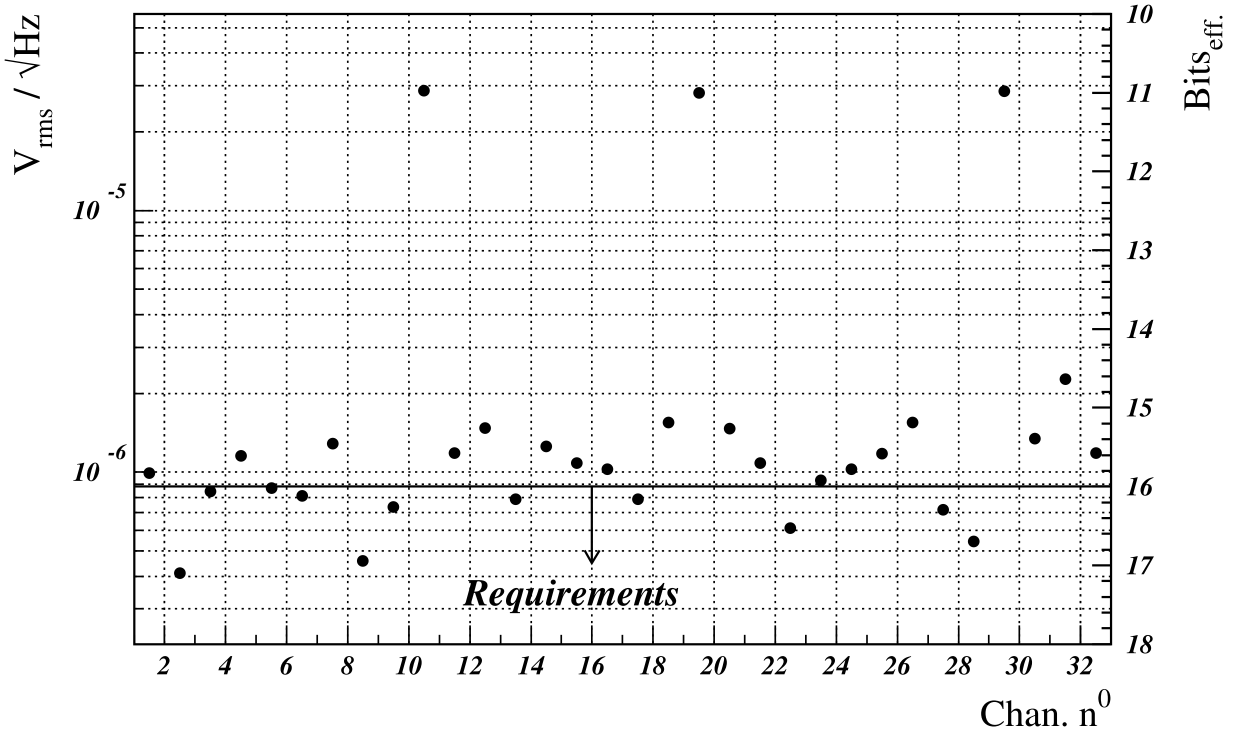

Figure 2: Amplitude Spectral Noise and Effective Bits as calculated from eq. (2), for the 32 channels (8 boards). Is also indicated the requirement effective Bits ≥ 16. The channels 10,19,29 suffer from readout errors.

3.2 Signal to noise ratio

A real estimation of the ADC effective bits comes from the noise level when a pure signal is converted to digital values. In that case, the noise is the background plus the quantization one. The number of bits is equal to the nominal one only if no background noise is present. The converters linearity could also be tested, if a signal of amplitude close to the ADC range is used. This input signal must be as close as possible to a monochromatic sinusoid, with a low frequency respect to the band extension. The time of measure must be as high as possible in order to minimize the out peak noise due to the finite signal duration. To match these requests we used a signal generator filtered by a resonant filter with:

- Resonance 474 Hz;
- Max gain 47 Db;
- Bandwidth (at -3 Db) 7 Hz;
- Max noise (at resonance) 13.8 $\mu V/\sqrt{Hz}$;
- Working gain $\simeq$ 37 Db;
- Working resonance noise 5 $\mu V/\sqrt{Hz}$;
- Attenuation at ± 200 Hz from the resonance: 28 Db.

We formed a filtered signal of amplitude ± 9.7 V (6.9 V_{eff}), put into some ADC channels. Its configuration and test run conditions have been:

- ADC input range: $A = \pm 10\ V$;
- 32 channels readout;
- Sampling frequency: $F_s = 20\ KHz$;
- Flip/Flop frequency: $F_f = 10\ KHz$;
- Time of measure 3.5 s (70000 data);
- FFT on 65536 points (bin width 0.3 Hz);
- Hanning window;

In the pictures below are shown the low frequency parts of typical amplitude spectra, first of the master channels and second of the slave ones.

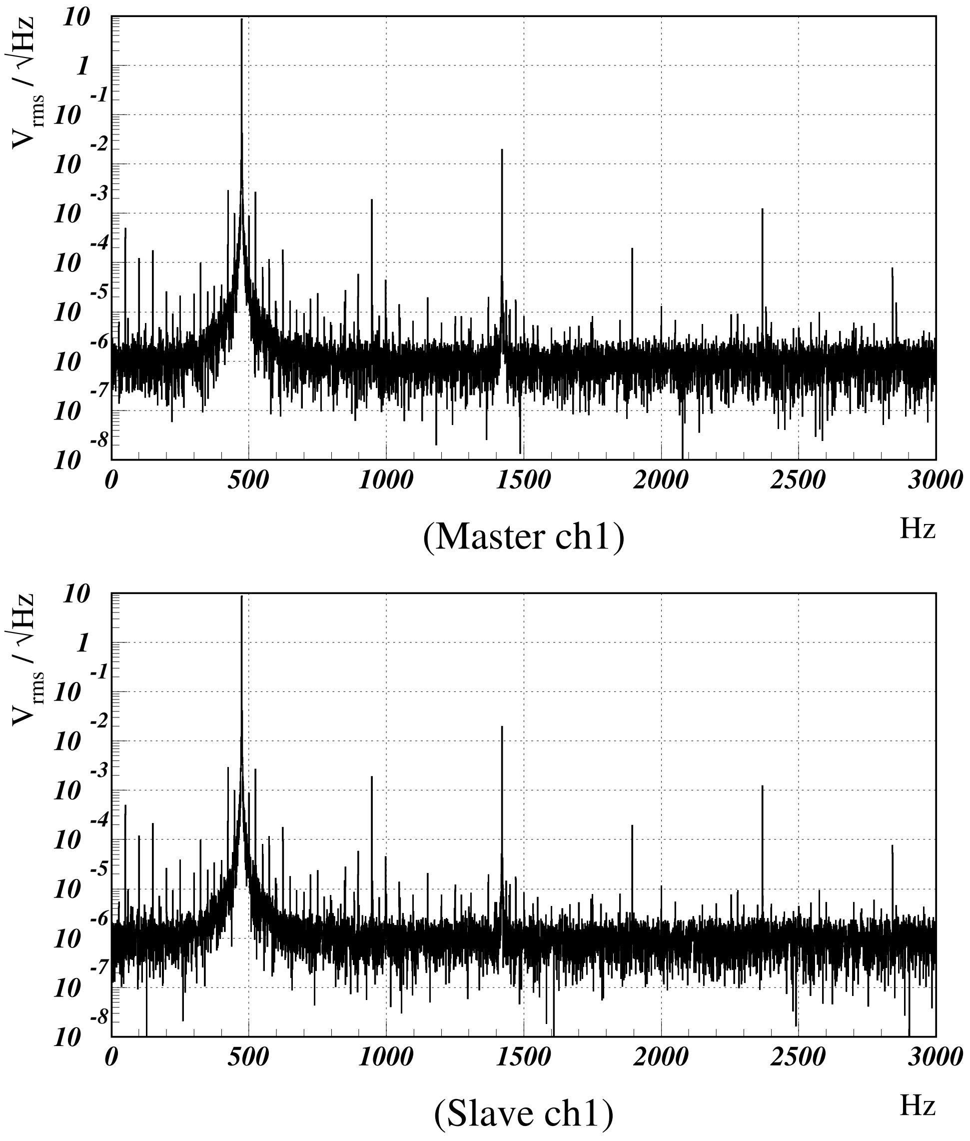

Figure 3: Low frequency zoom of the amplitude spectrum for the 1^{st} channel of the master board (up), and for the 1^{st} channel of a slave (down), with 6.9 V_{rms} input.

It's well visible the 948 Hz harmonic at -74 Db and the 1422 Hz harmonic, superimposed to the unknown peak at ~ 1420 Hz. We still did not determin if these harmonics were due to the input signal or to the ADC.
The use of the Hanning window permits to reduce the signal truncation noise below the level we want to measure. Otherwise (rectangular window) such noise should be one order of magnitude over the ADC one.

We can now sum up the results for the measured quantization noise:

1. The noise floor is near the background one. Its mean value is 1.44×10^{-6} $\frac{V_{rms}}{\sqrt{Hz}}$;
2. The number of effective Bits (mean value) is 15.28;
3. The first harmonic distortion is less than -70 Db;
4. The Signal to Noise Ratio (SNR), that we express as $\frac{\sigma_{in}}{\sqrt{S_{xx}} \times \sqrt{\Delta\nu}}$ to not depend on the peak resolution, is $SNR = 8.75 \times 10^6$;

3.3 Cross-Talk

We take the data with the same frequency as before, with ± 9.7 V in the channel 1 and the other three closed on 50 Ω. We make an FFT on 8192 points (8 spectral averages), windowing with Hanning, in order to detect possible cross talk between the channels.
In the next picture (fig. 4 on next page) we have plotted the amplitude spectra of 3 channels of the same board. As we can see, the ratio of the induced signal to the input, at the frequency 475 Hz, is about -115 Db for the ch. 4, and -120 Db for the ch. 2 and 3.

3.4 Results

Here we can finally summarize the results of these preliminary tests made on the ADC 4ch. mod. Etep 264A-265A:

- Background noise is below the requirements: its mean value on the channels free from errors is ($\overline{N}_{eff} = 15.8$);
- Not acceptable errors are still present: the nature of these errors are currently under investigation;
- Effective bits with signal (mean value) $\simeq 15.3$;
- Harmonic distortion: ≤ -73 Db;
- Unidentified peaks at $1420, 2840$ Hz;
- Noise peaks at $F_b, F_{b/2}$ (only on the slave boards);
- Cross-talk between ch. 1 and 4: ≤ -115 Db;
- Cross-talk between ch. 1 and 2,3: ≤ -120 Db.

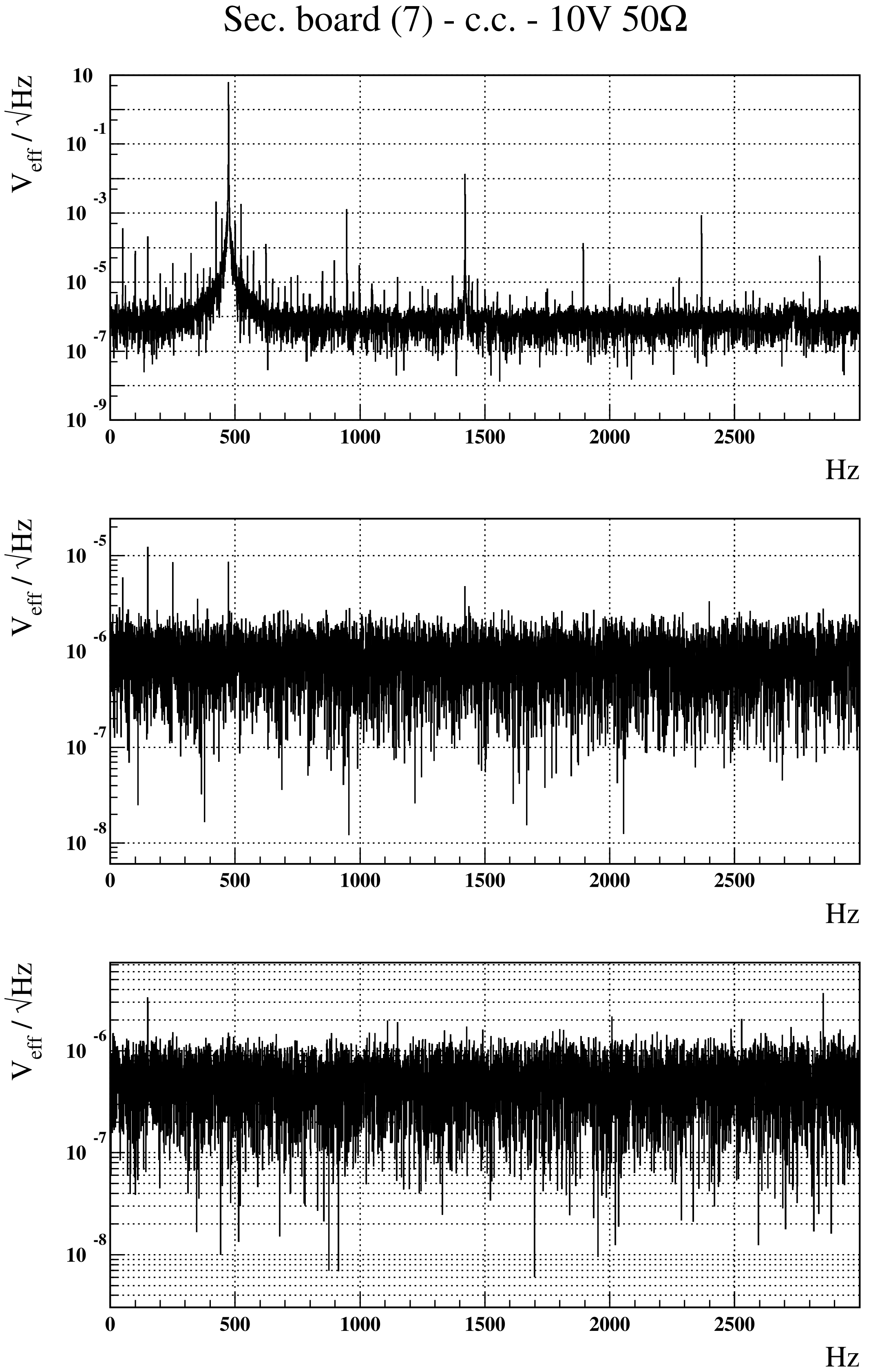

Figure 4: Amplitude Spectrum for 1^{st} channel (up, with signal), 4^{th} (in the middle, with 50 Ω) and 3^{rd} channel (last one, with 50 Ω) of a slave board.

4 Low Cost ADC boards

As I said in the Introduction, the requirements on these boards are much less strict that for the four channels boards. We need more than 130 channels of this kind, distributed over the entire location. I present here some test, made on a 16 channel ADC board, entirely made by Etep, mod. 275NSY, that has a cost of about 1000 FF for channel.

4.1 Technical Feature

- 16 channels each board;
- Analogic-Digital converter 16 Bits;
- VME readout of 2-4-8 or 16 channels with block transfer procedure;
- Possible sampling frequency: between 8 KHz and 100 KHz with external trigger;
- Input signal range $\pm 10V$ (or $\pm 5\ V$ commutable by switch), limited at $\pm 8\ V$ on our board;
- External sampling and readout signals (TTL,1 to 10μs duration, synchronized);
- Two memory buffers, 256K-bytes each (up to 128.000 data for channel), changing with the acquire signal;

The acquisition strategy is the same of the 4 ch. type, but single boards are acquired through VME.

5 Tests

5.1 Background noise

This test has been run with:

- Analogic inputs closed on 50 Ω;
- ADC input range limited at $\pm 8\ V$;
- 16 channels readout;
- Sampling frequency: $F_s = 20\ KHz$;
- Flip/Flop frequency: $F_f = 100\ Hz$;
- Time of measure 3.5 s (70000 data);
- Analysis on 65536 points;
- FFT on 8192 points (8 averages);
- Rectangular window;

Here we report the spectra of the first four channels.

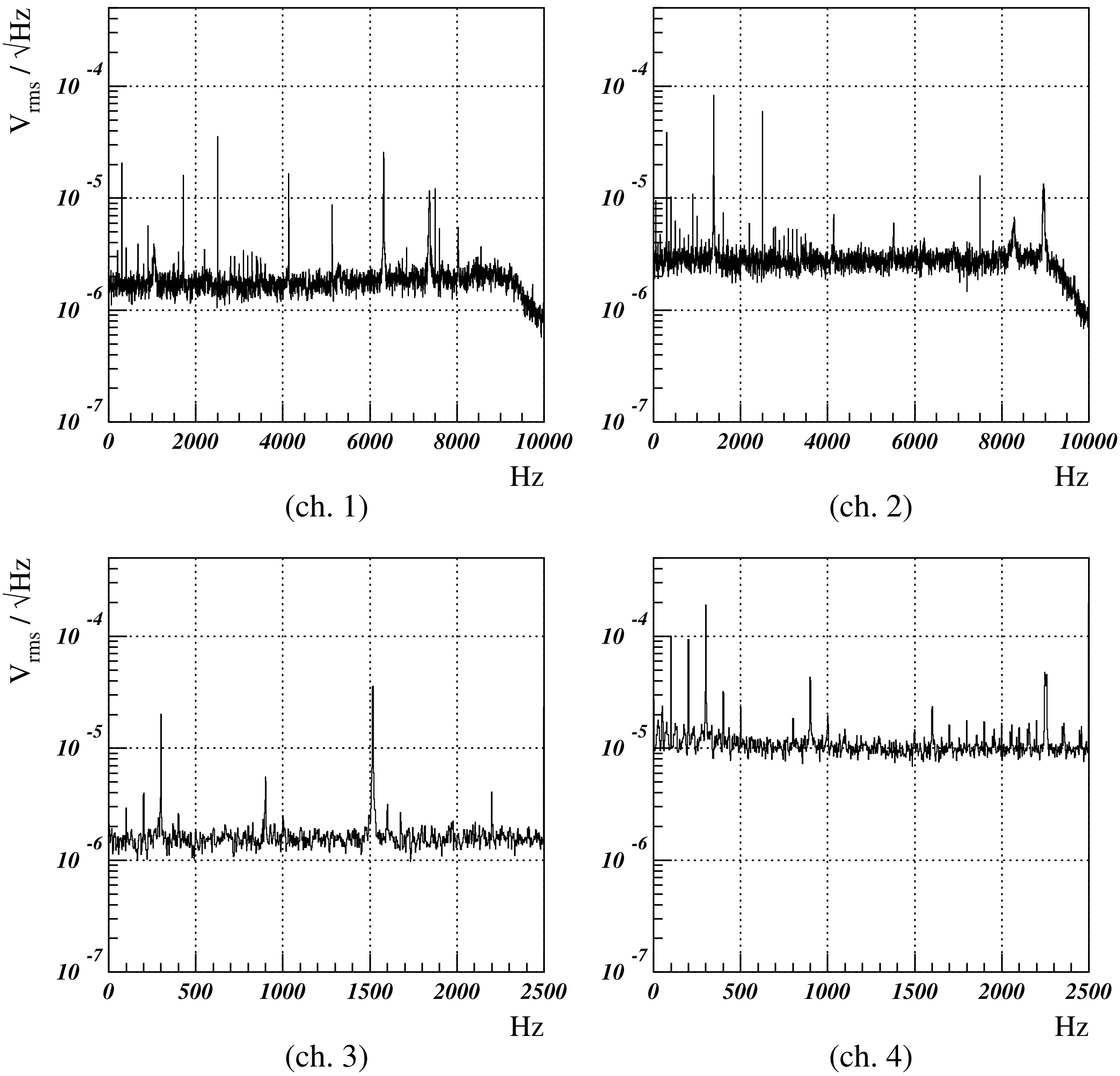

Figure 5: First four channels amplitude spectra. Up the channel 1 and 2. Down the low frequency part of the channels 3 and 4.

In the next page a summary of the noise mesure for the 16 channels of our test board is plotted.

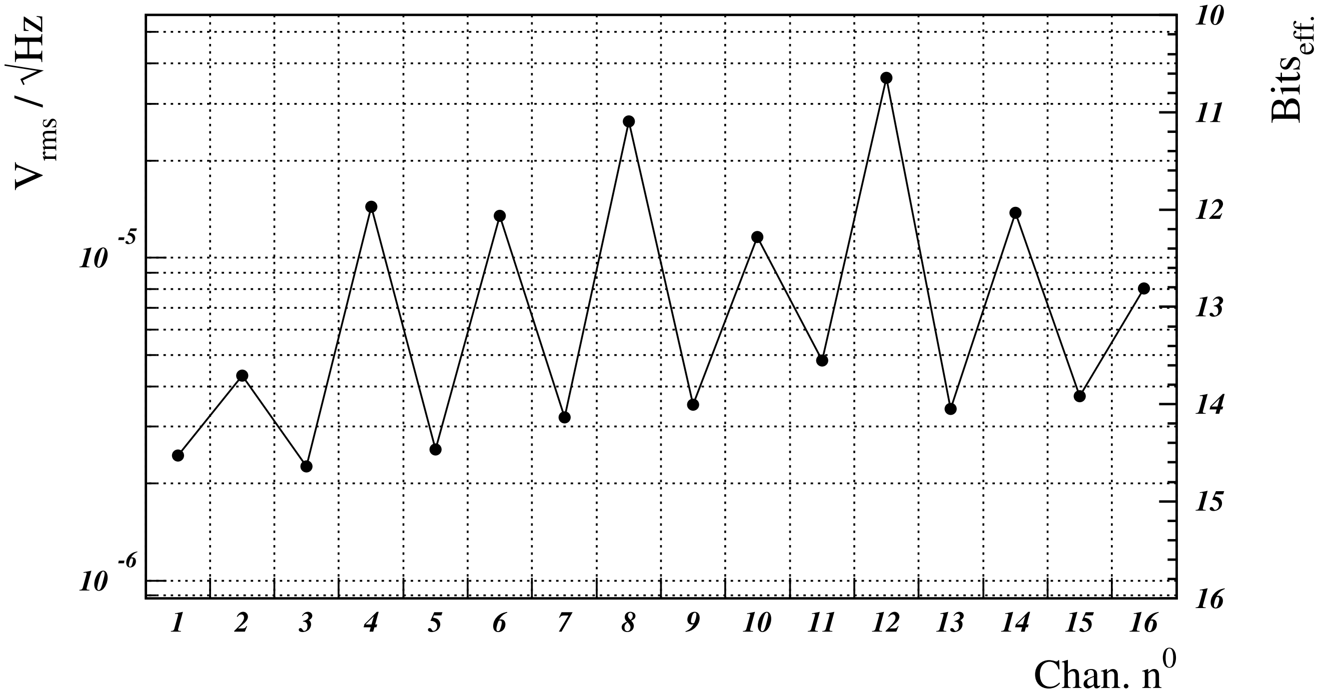

Figure 6: Amplitude Spectral Noise and effective Bits of the 16 channels.

5.2 Signal to Noise measurement

Again we summarize the test conditions and then plot an amplitude spectrum as example. The results of such test are summed up in the following section.

- Input signal amplitude $\pm 7.5\ V$ ($5.3\ V_{eff}$);
- Input signal frequency 475 Hz;
- 16 channels readout;
- Sampling frequency: $F_s = 20\ KHz$;
- Flip/Flop frequency: $F_f = 100\ Hz$;
- Time of measure 3.5 s (70000 data);
- Analysis on 65536 points;
- FFT on 65536 points (without averaging);
- Bin width 0.3 Hz;
- Hanning window;

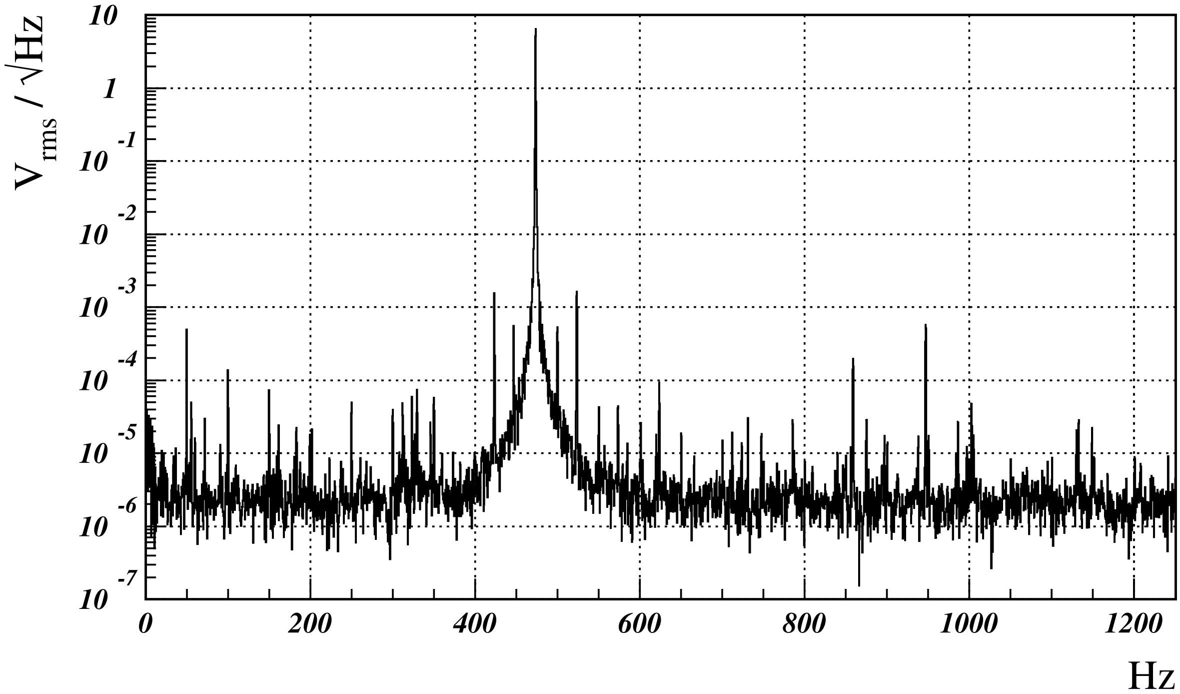

Figure 7: Low frequency part of the Amplitude Spectral Noise for channel 1.

5.3 Conclusions

- Asymmetry between even ($\simeq 12$ $bits$) and odd channels ($\simeq 14$ $bits$);
- Peaks at F_b and multiples (≤ 20 Db over the noise level);
- First harmonic distortion $\simeq -80$ Db;
- cross talk between odd ch. $\simeq -106$ Db;