CNRS

Centre National de la Recherche Scientifique

INFN

Istituto Nazionale di Fisica Nucleare

VME Crate List and Location

VIR-LIS-LAP-5000-108

Issue:1

Date: 24/10/97

VIRGO * A joint CNRS-INFN Project
Project Office: INFN-Section di Pisa*Via Livornese, 1291-56010 San Piero a Grado, Pisa.Italy.
Secretariat: Telephone.(39) 50 880 327 or 880352* FAX.(39) 50 880 350 * e-mail virgo@Pisa.infn.it

CHANGE RECORD

Issue/Rev	*Date*	*Section affected*	*Reason/ remarks*
issue 1	23/10/97		

Authors:	**Date**	**Signature**
B. Mours		
Approved by:		

TABLE OF CONTENTS

1. INTRODUCTION

It this work document we first try to summarized all the VME crates and their content. The goal is to check that there is no missing hardware or double count. This will be also very useful to cross check the interface between the crates and also the physical location of each crate. Then the list of slow monitoring station is given. Finally, the workstations with their location and their first assignment are presented. Please notice that since the exact design of each crate is not completely frozen this list will still evolve.

2. CRATE CONTENT

The content of each crate is given bellow. In this list the following hardware is used:

- VME crate 21 slots 9U (basic package reference: 70-204-45 from ELMA). Power supplies 500W (+5V/80A; +12V;10A; +12V/2A; -12V/10A), Automatic daisy chain, J1 and J2. Cooling with 3 fans.
- VME Crate 7 slots 4U (basic package reference: 70-204-25 from ELMA). Power supplies 250W (+5V/40A; +12V;6A; -12V/2.5A). Automatic daisy chain, J1 and J2. Cooling with 1 fan.
- CPU: 604 from CETIA or CES (RIO2-8062FA)
- Timing: board from LAPP
- TTL/OPTO and OPTO/TTL: copper to fiber converter for timing signals
- GPS: BC637-VME from Bankcom
- DOL: board from LAPP
- ADC: ADC-4c: 4 channels ETEP-264 board: 2 slots
  ADC-16c: 16 channels ETEP-298 board: 2 slots
  ADC-P: board from PISA
  ADC-M: 8 channels M module from Orsay
- DAC: DAC-P: 8 channel board from PISA
  DAC-M: 8 channels M module from Orsay
  DAC-A: 4 channels DAC board 704 from ADAS with 32k FIFO
- DSP: DSP board from Pisa
- PVIC: Mirrored memory board from LEXAN, CES or VMIC (TBD)
- M-Module Mother board from xxx
- Rack: 42U rack from ATOS

The lab responsible of each crate is also given.

2.1. Control Building:

C1: Timing (21 slots, 13 used)(Annecy)
- 1 CPU-16M (slow control),
- 2 GPS,
- 2 Timing,
- 4 TTL/OPTO,
- 4 OPTO/TTL

C2: Slow Monitoring Frame Builder (Annecy)(7 slots, 3 used)
- 1 Timing,
- 1 CPU-16M (ethernet IO, PCI connection usefull)
- 1 DOL to Man frame Builder

C3: Main Frame Builder (7 slots, 6 used)(Annecy)
- 1 CPU-64M (large memory, intensive IO, little computation, PCI connection needed),
- 4 DOL,
- 1 PVIC (to data distribution)

C4,5: Raw data archiving (7 slots)(Napoli) **(TBC BY F. BARONE)**
- 1 PVIC
- n CPU (n from 1 to 6)

C6: Data quality and online monitoring(Annecy)**(TBC)**
- 1 PVIC

1 CPU-16M (or one workstation with PCI slot)

C7: Trigger (Annecy)**(TBC)**

1 PVIC,
1 CPU-128M for h reconstruction and data buffer (intensive IO)
n CPU-16M for algorithms (n around 5)(intensive computation, PCI connection needed?)

C8: Global control monitoring (Orsay)**(TBC)**

1 PVIC
1 CPU-16M (or one workstation with PCI slot)

2.2. Main building:

C21: Laser control (21 slots)(Orsay)

1 CPU-16M,
5 ADC,
1DAC (m), 2 Serial lines control (m), 1 Status register (m)
1 Command register(m), 2 Timer-Gate(m),
1 Timing
VSB 2 Cameras for mode control
1 CPU-32M (intensive computation and IO)

C22: Auto Alignement 1 (7slots)(Orsay)

1 CPU-16M,
ADC (?),
1 DAC (m), 1 Timer-Gate(m), 1 Status register (m), 1 Command register(m)

C23: Auto Alignement 2 (7slots)(Orsay)

1 CPU-16M,
ADC (?),
1 DAC (m), 1 Timer-Gate(m), 1 Status register (m), 1 Command register(m)

C24: MEB: entry bench position (21 slots)(Orsay)

1 Timing
1 CPU-16M,
1 Camera,
1 DAC(m), 1 Timer-Gate(m), 1ADC, 1 Status register (m),
1 DOL to Suspenssion control,

C25: Detection bench control (21 slots, 12 used)(Annecy)

Task: Mode cleaner locking
1 Timing,
1 CPU-16M (mode cleaner locking, photodiodes, picomotor and fast shutter control)
1 ADC-16C mode cleaner control (2 diodes before and after: Phase and DC: 8 channels
2 temperature)
1 DAC-P mode cleaner temperature control
VSB 3 Cameras for beam imaging,
1 CPU-32M (intensive computation and IO)
3 DAC-M Photodiodes control: Vbias and delay, 25 channels, 12 bits, slow
1 DAC-M Fast shutter control, 2 or 3 channels, 12 bits, slow
1 RS232 for picomotor control (New Focus or modified timing board ??)
1 DOL to local frame builder

C27: Photodiodes readout D1: (21 slots, 20 used)(Annecy)

1 Timing,
1 CPU-16M,
1 DOL to local frame builder,
1 DOL to crate diode readout D5,
8 ADC-4c: 16 diodes (phase and quadrature signals)

Nota: C27,28 and 29 need a 3 U additional power supply

C28: Photodiodes readout D5: (21 slots, 16 used)(Annecy)

1 Timing,
1 CPU-16M,
1 DOL to local frame builder,
1 DOL to Global Control
1 DOL from crate diode readout D1,
1 DOL from crate diode DC,
5 ADC-4c: 2 diodes D1', 2 diodes D1", 2 diodes D2, 2 diodes D5 (P,Q)
2 diodes D2' = 20 channels

C29: Photodiodes readout DC: (21 slots, 18 used)(Annecy)
1 Timing,
1 CPU-16M,
1 DOL to local frame builder,
1 DOL to crate diode readout D5
7 ADC-4c:16 diodes D1, 2 D1', 2 D1", 2 D2, 2 D5, 2D’2 (DC) = 26 channels (or

C30,31,32,33: Signal detection for detection bench (Annecy)
Analogic electronic (8 diodes per crate)

C34: Alignment readout (21 slots, 8 used)(Annecy)
1 Timing,
1 CPU,
1 DOL to global control,
1 DOL to Frame Builder,
2 ADC-16c (6 quadrant diodes at < 1 kHz(TBC)) (ADC-4c needed ??? to be checked)

C35: Alignment(**Frascati)**
Analogic electronic

C36: Global Control (21 slots) (Orsay)
1 Timing,
2 or 5 CPU (control &signal processing),
1 DOL to Local Frame Builder,
4 DOL from diodes readouts
1 DOL from laser
6 DOL to suspension controls

C37: Calibration (7 slots, 5 used)(Annecy)
1 CPU-16M (control &signal processing),
1 GPS (to generate the clock and get the abolute timing of the generated signal)
1 DAC-A (2 signal at 20 kHz for laser diodes, 2 for coil control)
1 ADC-16c (to readout 2 quadrant diodes par mirror = 16 channels)

C38: Environement & building control (21 slots?) **(TBD BY F. Barone)**(Napoli)
1 CPU-16M, dedicated network hardware

C39: Local readout (21 slots, 12 used)(Annecy)
1 Timing,
1 CPU-16M,
1 DOL (to local frame builder),
1 GPS to record the absolute time
4 ADC-16c: 8 acoustic noise, 8 em moise, 5 line voltage, 4 calibrations (@ 20kHz)
8 x 3 seismic noise (@ 1kHz)
x for laser data acquisition

C42,44,46,48,50,52: Suspension control (21 b.) (Pisa)
1 Timing
1 CPU-16M (intensive computation and IO)
1 Digital I/O to controls the upper part control
VSB 1 DOL from Global control or Bench control
1 DSP for mirror control
1 DAC-P to Marionetta control
1 DAC-P to reference mass control

1 DOL to local frame builder
VSB 1 or 2 Cameras for local position measurement,
1 CPU-32M (intensive computation and IO)
VSB 1 DSP for upper stage damping
2 ADC-P for accelerometer readout
2 DAC-P to upper coils contrl control
Dual port RAM board ? (TBC)

C41,43,45,47,49,51,53: Suspension Analogic Electronic (Pisa).
We have 2 NIM crate (a and b) in the DAQ room crates per suspension
(40,41 is for the input bench; 42,43 for the power recycling; 44,45 for the beam splitter;
46,47 for the west input mirror 48,49 for the north input mirror 50,51 for the detection banch;
52,53 for the signal recycling)

For each Suspension, we will have near the tower (Pisa):

- 1 NIM crate
- 3U for the preamplifier
- 3U for the suspension motor control

For each suspension, we will have in the DAQ room 1 U for the marionatta motor control (Roma)

C54: Timing (21 slots, 17 used, no VME signal used)(Annecy)
16 OPTO/TTL
1 TTL/OPTO: return to central timing
1 TTL/OPT for 6 MHz modulation signal and alignement modulation signal to end mirror

C55,56: Local Frame Builder A and B (21 slots, x used)(Annecy)
1 CPU-32M (large memory, intensive IO, little computation, PCI connection needed),
n DOL from local readout and controls,
1 DOL to main frame builder,

C57: Imaging readout (7 slots, x used)(Annecy)
1 Timing
1 CPU-32M (intensive computation and IO)
n Cameras,

C58: OS9 Boot Processor
1 CPU

C59: Suspension auxiliary devices (21 slots)(Pisa)
1 CPU-32M
Boards needed for the suspension temperature control

2.3. Mode cleaner:

C61: Local readout (7slots, 5 used)(Annecy)
1 Timing,
1 CPU-16M,
1 DOL (to local frame builder)
1 ADC-16c to read: 2 acoustic noise, 2 em moise, 2 line voltage (@ 20kHz)
2 x 3 seismic noise (@ 1kHz)

C62: Mmc-CPM: mode cleaner mirror position (7 slots)(Orsay)
1 CPU-32M,
1 Camera,
1 Status-M, 1 Timer-Gate(m),
1 DOL to Suspenssion control,
1 Timing

C63: Mmc-CLM: mode cleaner mirror position (7 slots)(Orsay)
1 CPU-32M,
1 Logic-control-M, 1 Timer-Gate(m),

2 DOL to Suspenssion control,

C64: Suspension control (21 slots)(Pisa)
1 Timing
1 CPU (intensive computation and IO)
1 Digital I/O to controls the upper part control
VSB 1 DOL from input Bench control
1 DSP for mirror control
1 DAC-P to Marionetta control
1 DAC-P to reference mass control
1 DOL to local frame builder
VSB 1 or 2 Cameras for local position measurement,
1 CPU (intensive computation and IO)
VSB 1 DSP for upper stage damping
2 ADC-P for accelerometer readout
2 DAC-P to upper coils contrl control

C64: Suspension control (Pisa)
Analogic electronic

C65: Timing (7 slots, 5 used, no VME used)(Annecy)
4 OPTO/TTL
1 TTL/OPTO: return to central timing

The crates will be installed in 2 racks. One for the suspension electronic. The other one for the timing, local readout and the mode cleaner mirror position.

2.4. End building:

C71: End mirror bench control (long. signals & alignment)(21 slots, 14 or 15 used(Annecy)
1 Timing
1 CPU-16M (control & signal processing),
1 DOL (to global control),
1 DAC-M for diode control (Vbiais, delay)
2 ADC-4c for longitudinal diodes readout (2 diodes=6 channels)
1 ADC-16c for the 2 quadrant diodes readout
2 OPT/TTL for 6 MHz modulation signal and alignement modulation signal
VSB 1 or 2 Cameras for beam shape control and initial alignment,
1 CPU-32M (intensive computation and IO)

C72: Signal detection(Annecy-Frascati)
Analogic electronic

C73: Environement & building control(Napoli)
1 CPU-16M (control), dedicated network hardware

C74: Local readout (Annecy)
1 Timing,
1 CPU-16M,
1 GPS to record the absolute time
1 DOL (to local frame builder)
1 ADC-16c to read: 2 acoustic noise, 2 em moise, 2 line voltage (@ 20kHz)
3 x 3 seismic noise (@ 1kHz)

C75: Suspension control (21 b.)(Pisa)
1 Timing
1 CPU-16M (intensive computation and IO)
1 Digital I/O to controls the upper part control
VSB 1 DOL from input Bench control
1 DSP for mirror control
1 DAC-P to Marionetta control
1 DAC-P to reference mass control

⌊ 1 DOL to local frame builder
⌈VSB 1 or 2 Cameras for local position measurement,
⌊ 1 CPU-32M (intensive computation and IO)
⌈VSB 1 DSP for upper stage damping
| 2 ADC-P for accelerometer readout
⌊ 2 DAC-P to upper coils contrl control
C76,77: Suspension Analogic Electronic (Pisa). 2 NIM crates

In addition, we will have near the tower (Pisa):
- 1 NIM crate
- 3U for the preamplifier
- 3U for the suspension motor control

We will also have 1 U for the marionatta motor control (Roma)

C78 Timing (7 slots, 5 used, no VME used)(Annecy)
4 OPTO/TTL
1 TTL/OPTO: return to central timing
(crate number are given for the north arm. Add 10 to get crate numbers for the west arm)

3. The list of Slow Monitoring Stations

Here is the list of the foreseen slow monitoring station with there name:

Tube control station:	TW01,TW02,...TW11,TN01,...TN11 (for west & north arm)
Tower control:	TOIB (input bench), TOMC (mode cleaner),
	TOPR (power recycling), TOBS (beam splitter),
	TOIN (input mirror north), TOEN (end mirror north)
	TOIW (input mirror west), TOEW (end mirror west)
	TOSR (signal recycling), TODB (detection bench)
Building control:	BCCE (for central building), BCMC(for mode cleaner)
	BCEW (for end west), BCEN(for end north)
Environment monit:	EMCE (for central building), EMMC(for mode cleaner)
	EMEW (for end west), EMEN(for end north)
Laser control:	LASR
Benchs:	IBEN (input), DBEN (detection), NBEN (north arm bench),
	WBEN (west arm bench)
Calibrator:	CALI

4. Workstations Implementation

4.1. Control Room & Computer Room

The Control room will contain two clusters of identical workstations. Even though they will be able to run any user interface they will be dedicated to one or two specific type of control. Two clusters will be used instead of one in order to do system maintenance without stopping VIRGO. Here is the list of the foreseen workstations:

- W1: Tube control & Tower control (on slow mon. net.)
- W2: Building control & Environment control (on slow mon. net.)
- W3: Laser & input bench control
- W4: Detection bench control & Signal detection
- W5: Suspension control
- W6: Locking & Linear alignement
- W7: Name Server, Supervisor & Timing control
- W8: Non Linear Alignement & Beam Imaging
- W9: Local Readout & Frame Builder
- W10: Data distribution control & Data archiving
- W11: Trigger control & Data Monitoring

- W12: Data distribution: This workstation is located inside the computer room.
  It is a more powerful workstation with lot of disk space and special hardware.
- W13: Network analyser
- W14: Software distribution

The rack content is the following:

- R1 Cabling arrival
- R2 Network Hardware
- R3 Crate 1, 2, 3, 6, 7, 8
- R4 Crates 4,5
- R5 Alpha server

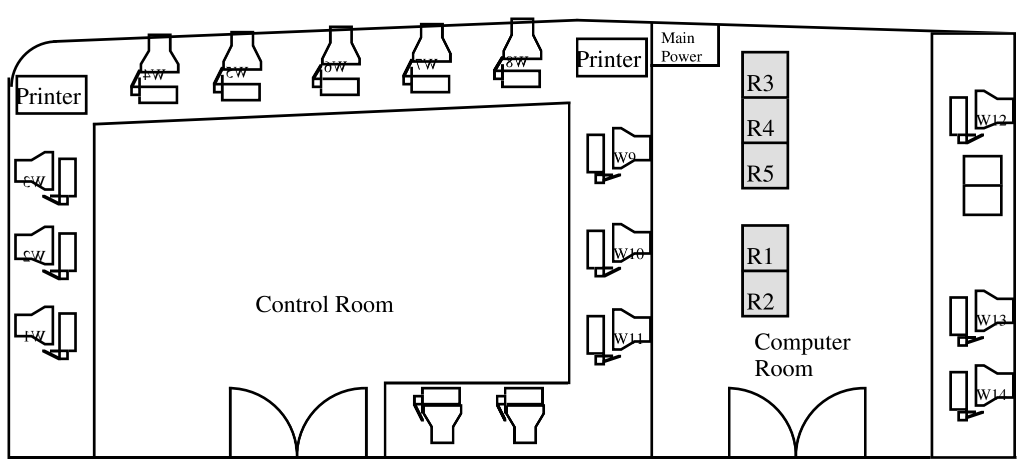

Figure 1 Control Room and Computer room. Video monitor (for beam imaging or for room survey) will be installed above the workstation

4.2. Main Building

A few workstations (or X terminal) will be available in the Data acquisition room to locally work on the control. They will be on the same cluster as those in the Control Room. Here is the list:

- W21: Tower control & Tube control (on slow mon. net.)
- W22: (for W3,W6)
- W23: (for W4)
- W24: (for W6)
- W25: (for W8)

The rack content is the following:

- R11 Cabling arrival
- R12 Network Hardware
- R13 Crates C30,31,32,33 Analogic electronic for detection bench (TBC)
- R14 Crates 25, 50,51a,51b, Detection Bench ctrl , Detection Bench Suspension control
- R15 Crates 27,28,29 Photodiode readout (longitudinal)
- R16 Crates 34,35,57 Photodiode readout (alignment) Imaging,
  Patch Panel for coax (6U)
- R17 Crate 54,55,56,36 Timing and Frame Builders, Global Control
- R18 Crates 37,39,38 Calibration, local readout, Env. monit & Build control

- R19 Crates 46,47a,47b,59 Input West Suspension control, Temperature control
- R20 Crates 48,49a,49b Input North Suspension control
- R21 Crates 44,45a,45b Beam Spliter Suspension control
- R22 Crates 42,43a,43b Power recycling Suspension control
- R23 Crates 40,41a,41b Input bench suspension control
- R24 Crates 21,22,23,24,58 Laser and Input bench control, OS9 boot
- R25 Patch Panel for Laser and Input bench control

(depending of the size of a NIM crates, 2 suspension control may be group in one rack).

The crates for the

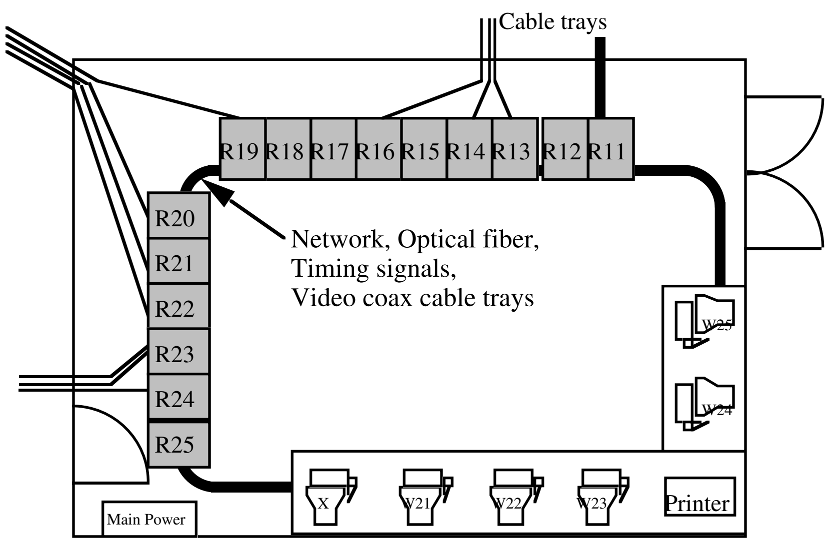

Figure 2 Control Room and Computer room. Video monitor (for beam imaging or for room survey) will be installed above the workstation. There will be one cable tray per tower to groupe all the cables (suspension, environment monitoring, calibration, camera, monitor, local ethernet?)

The electronic of the end of arm for the central interferometer will be installed near each optical bench.

A first estimation for the length of the cable used by the camera is the following:

Cables length: (DAQ room+cable tray + around the tower)	
Detection Bench	3m + 11.5+3m = 20.5m
Detection Tower	3m + 10.5+3m+4m = 20.5m
Recycling Tower	4.5m + 4.5+1.7m
Input Bench Tower	3m + 4.5+1.7m + 4m = 13.2m
Beam Splitter Tower	4.5m + 5.5+7 + 4m = 15.7m
West Tower	4m + 10.5+1.7m + 6m = 22.2m
Nord Tower	4m + 12.5+1.7m + 4m = 22.2m
West optical table	6m (the crate is near the table)
Nord optical table	6m

4.3. Mode Cleaner or End Mirror Buildings

Two X Termnial will be available next to the tower. There will be also one rack with 2 crates for the suspension control and one for the timing and the local readout.