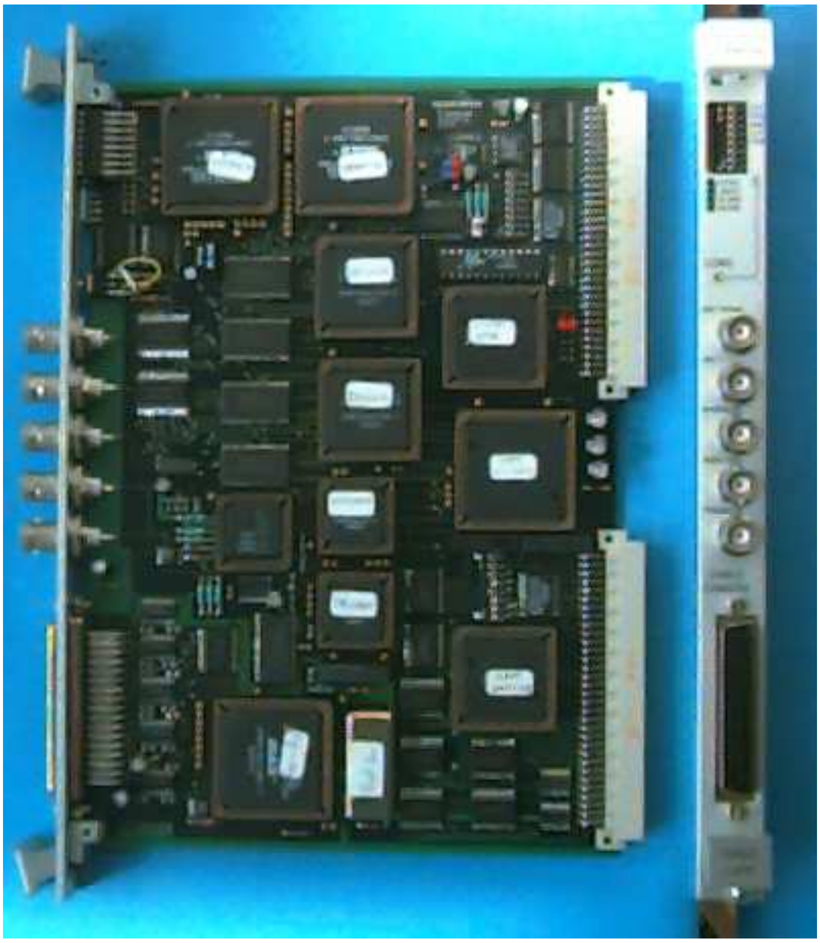
A VME/VSB board for real-time positioning and image analysis

Applications:

- real time monitoring and positioning.
- image analysis.
- fast feedback loop.



Interfaced to a digitital camera:

- 512x512 pixels.
- 20 MHz pixel clock.
- ADC converter (8 - 10 bits).
- asynchronous mode: external trigger control.
- framestore grab signal.
- mixed video blanking signal.

Key features:

- Storage and readout from memories are synchronized with the 20 MHz pixel clock.
- VME bus and VSB private bus.
- Block transfer can be used for higher readout rate.
- External trigger input to synchronize image capture.
- Integration time and gain control for different light level conditions.
- Interruptions generation for external device synchronization.

Specifications

Video synthesis:

- **Non interlaced CCIR format** in 256x256 pixels.
- Data stored in a 64 Kb memory (TC558128) before reconstruction.
- Synchronization and blanking signals provided through programmable logic devices (Altera MAX 7000 family).
- DAC (Bt121) with composite video output and 75 ohm adaptation.
- Continuous memory readout at 5 MHz.

Memorization module:

- **512 Kb memories** (TC558128) for pixels storage on **16 bits dynamics**.
-**Acquisition synchronized with pixel clock**.
- Read/write multiplexing on the two clock phases.
- **Sequential readout on 32 bits** (four or two pixels) with reading counter increment at each end of VME cycle.
- Read counter address programmable through VME or VSB bus for access on limited image area.
- Writing memories tests through VME or VSB.
- Continuous memories readout at VME cycle rate.

Synchronization and controls:

- Uses **pixel clock at 20 MHz** provided by the camera.
- **External or internal trigger** at 60 Hz maximum rate.
- **Integration time control** between 100 µs and 1s.
- **Gain control** by a 12 bits DAC_B to apply a voltage between 0 and +10V (+20 dB).
- Other 12 bits DAC_A output available in front panel.
- **End of frame signal** output in front panel.
- **Frame counter**.

VME VSB modules:

- **Slave device**: (A24/D32 or A32/D32) for VME on P1, P2 connectors. (A32/D32) for VSB on P2 connector.
- **VME address**: 20 LSB programmed in logic device. 12 MSB set by slots on the board.
- **VSB address**: programmed in logic device.
- Mapping: the board is reserved with a read/modify/write cycle mode (by setting a byte at the board address).

Format	base address
VME A24/D32	0x0* **** to 0xF* ****
VME A32/D32	0x000* **** to 0xFFF* ****
VSB A32/D32	0xC00* **** to 0xCFF* ****

- **Interruptions generator** on level 1 to 7 (the level is set by slots on board, default is level 5). An interruption vector register is included for interruption source identification. The interruption request can be generated at any end of line stored in memory. This line number is programmable through VME. The impulsion request is also available at a BNC output in front panel.
-**(FR/FW)** memories read/write and programmable registers, functions generator (coding at base address + offset):

Labels	offset	comment
FR0 - FW0	0x00	read/write reserved board - 8 bits
FR3	0x04	read status register - 16 bits
FW3	0x04	write command register - 16 bits
FR2	0x08	read frame counter - 16 bits
FW2	0x08	load read counter address - 17bits
FW9	0x0C	load veto strobe register - 10 bits
FW8	0x14	load interrupt vector - 8 bits
FW7	0x18	load integration time - 15 bits
FW6	0x1C	load interrupt line number - 10 bits
FW4	0x20	load DAC_A - 12 bits
FR1 - FW1	0x80000	read/write memories

Command register:

- Programmable by loading a word through VME or VSB, or by loading a configuration (8 LSB) set by switches in front panel.

C0 = 0 : pixel acquisition off .
= 1 : pixel acquisition on.

C1 = 0 : external trigger.
= 1 : internal trigger.

C2 = 0 : VME or VSB read.
= 1 : VME or VSB write.

C3 = 1 : reset.

C4 = 0 : camera alimentation off.
= 1 : camera alimentation on.

C5 = 0 : 4 pixels readout on 32 bits.
= 1 : 2 pixels readout on 32 bits.

C8 = 1 : alimentation test (+12V and +5V).

C9 = INTEN = 0 : interrupts desable.
= 1 : interrupts enable.

C10 = LBUSY - C11 = SLVME - C12 = SLVSB : VME or VSB bus busy.

C15 = RSBUSY = 1 : reset bus occupation.

Inputs - Outputs:

- Camera connector: female D50.
- Video output, external trigger input, interrupt request output, end of frame output, DAC_A output: BNC connectors.
- Load status register push button, switches, status on red LEDs.
- Green LEDs for bus signals.
- Differential buffer between camera and board.

Software

- Client - Server model :

C language and Motif under Unix and LynxOS.

Server: real time computation (positioning at 60 Hz max. rate). Gain and pedestal on image.

Client: image display: cuts, histograms, projections, zooms, 2D/3D representations, laser beam analysis: waist, modal decomposition. Camera and server configuration.

- Test program for board basic functions.

- Specific device driver for camera control and libraries for interruptions and block transfer (Available for LynxOS v2.1 or later).